ISSUED ON

11 OCT 2013

Part IB Paper 5: Electrical Engineering

LINEAR CIRCUITS AND DEVICES

Examples Paper 1 The Bipolar Transistor and Negative Feedback

Straightforward questions are marked †.
*Tripos standard questions are marked *.*

The Bipolar Transistor

1. The type BC107 silicon npn transistor has the dc characteristics shown graphically in Fig. 1. The transistor is to operate at the following working point:

$$V_{CE} = +10\,V, \quad I_C = 25\,mA, \quad I_B = 100\,\mu A, \quad V_{BE} = +0.7\,V$$

in each of the two circuits shown in Fig. 2.

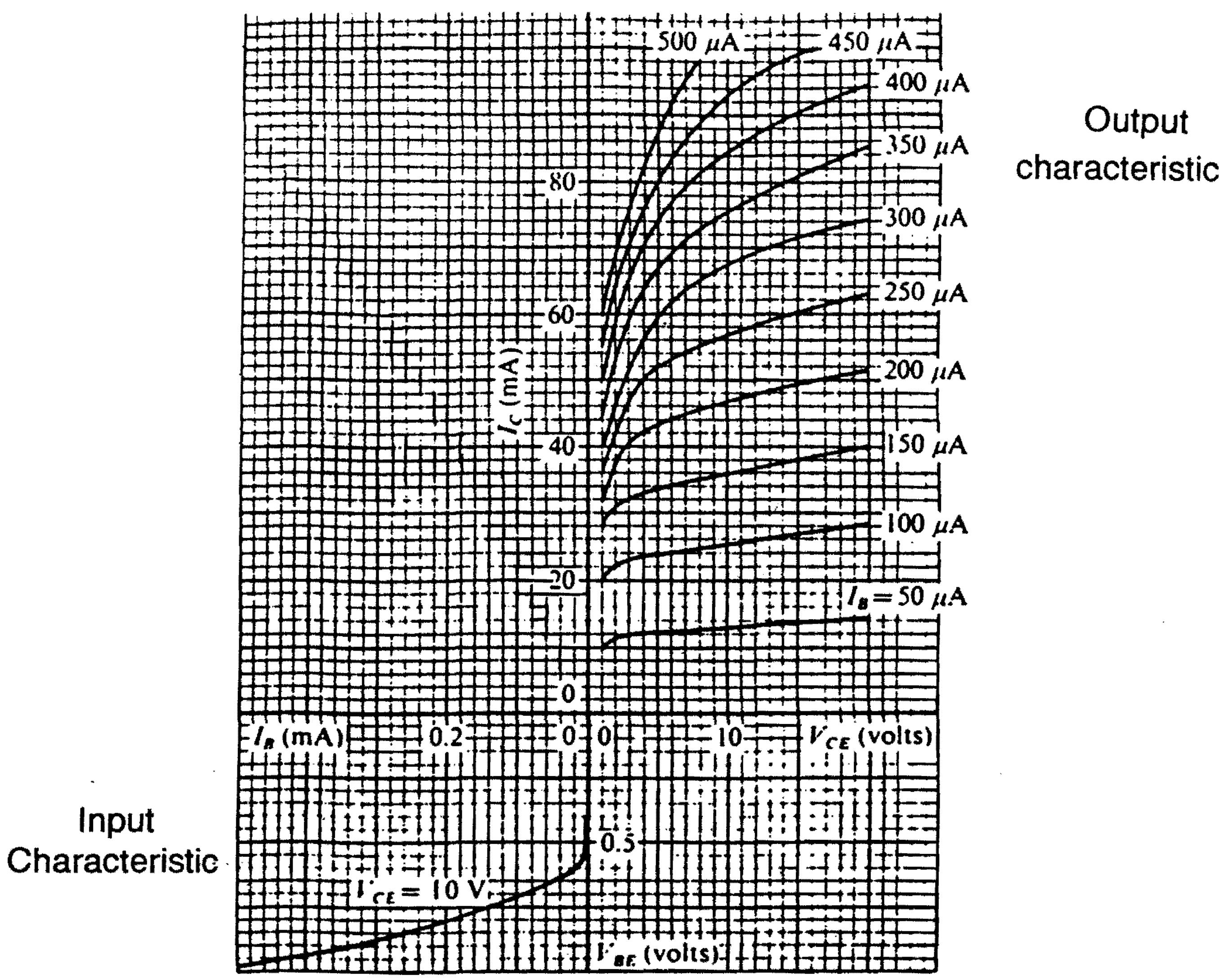

Fig. 1.

† (i) Find the values of R_1, R_2, R_3 and R_4 which will allow the working point to be attained in these circuits.

(ii) For the circuit of Fig. 2(a), draw a load line on the output I_C against V_{CE} characteristic. Estimate graphically the voltage gain of the amplifier for the operating region between $I_B = 50\,\mu A$ and $I_B = 150\,\mu A$.

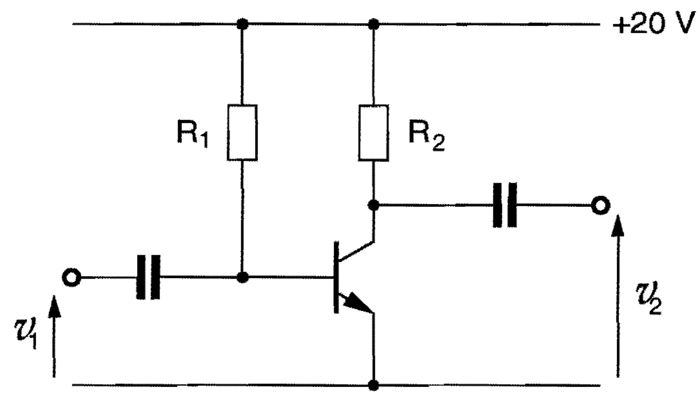

Fig. 2(a)

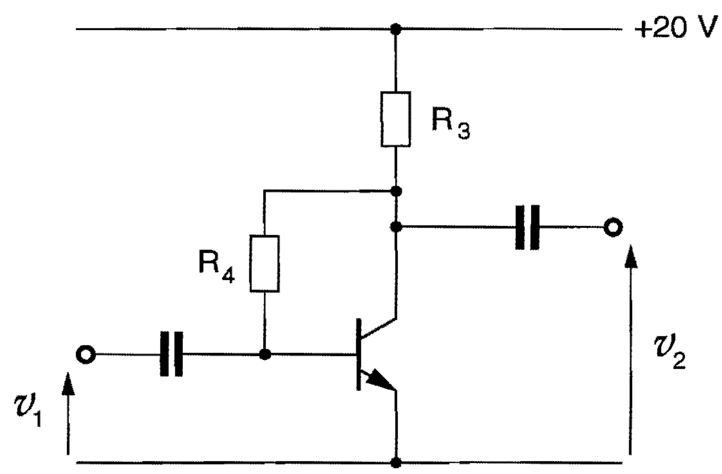

Fig. 2(b)

2. For the BC107 transistor operating at the working point described in Q.1, the effective small signal parameters are:

$h_{ie} = 1\,k\Omega$, h_{re} negligible, $h_{fe} = 250$, $h_{oe} = 300\,\mu S$

(i) Using this data, find the no-load voltage gain, input resistance and output resistance for the amplifier of Fig. 2(a) with $R_1 = 193\,k\Omega$ and $R_2 = 400\,\Omega$

*(ii) Estimate the input resistance of the amplifier shown in Fig 2(b), with $R_3 = 400\,\Omega$ and $R_4 = 93\,k\Omega$. Assume the gain is the same as for part (i).

3. In the 'Darlington pair', two transistors are connected, as shown in Fig. 3, to form a three-terminal device. If each of the transistors has negligible h_{re} and h_{oe}, show that the composite device has :

(i) an equivalent base circuit resistance of $h_{ie}(2 + h_{fe})$;

(ii) an equivalent current gain of $h_{fe}(2 + h_{fe})$.

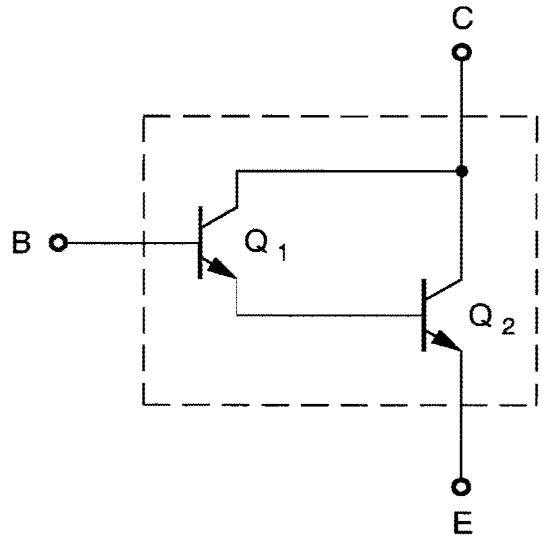

Fig. 3

4. A common-emitter amplifier is connected as shown in Fig. 4. The small-signal parameters of the transistor are:

$h_{ie} = 1\,\text{k}\Omega$, $h_{fe} = 50$, $h_{oe} = 25\,\mu\text{S}$, h_{re} negligible

Calculate the voltage gain $|v_2 / v_1|$, assuming that the reactances of the coupling capacitors are negligible.

* The high-frequency performance of this amplifier is limited by the collector-base junction capacitance, which in this case is 10 pF. Estimate the frequency at which the voltage gain is 70% of its low-frequency value. (Hint: neglect the effect of the capacitor current on the output circuit conditions, but include it when considering the small-signal voltage at the base).

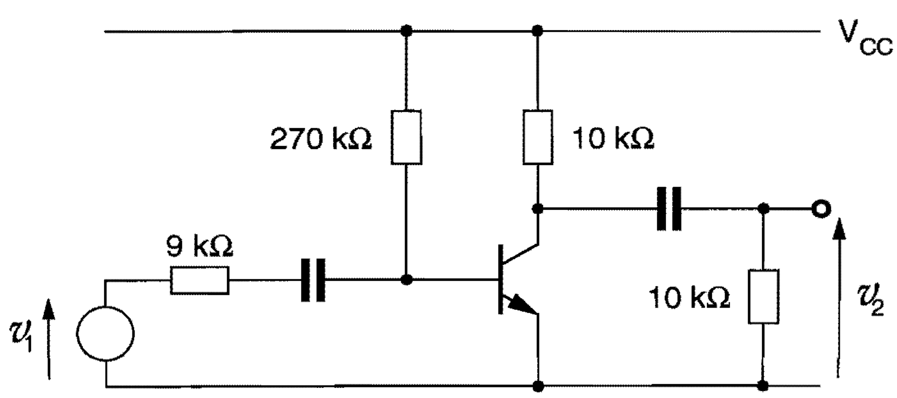

Fig. 4

5. Fig. 5(a) shows the circuit of a basic emitter follower, in which the transistor operates with $V_{CE} = 20$ V, if its dc current gain, $h_{FE} = 200$. Unfortunately, samples of the same transistor have values of h_{FE} in the range 100-500. Assuming the base emitter voltage V_{BE} is substantially constant at 0.7 V, calculate the possible range of V_{CE}.

The circuit of Fig. 5(b) is designed to stabilise the transistor working point, calculate the range of V_{CE} which can occur in this case. (You may find it helpful to reduce the base bias circuit to its Thevenin equivalent).

If the transistor has small-signal parameters:-

$h_{ie} = 1\,k\Omega$, $h_{fe} = 200$, h_{oe}, h_{re} negligible

find the amplifier input resistance for each circuit.

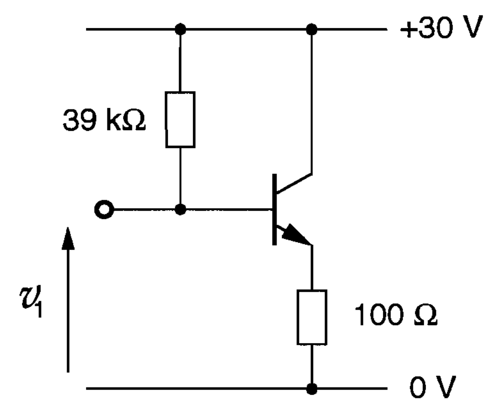

Fig. 5(a)

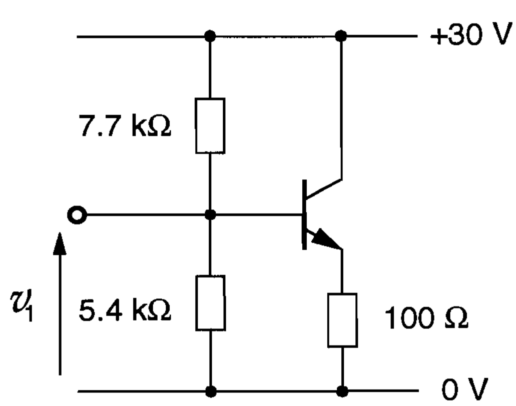

Fig. 5(b)

6. For the differential amplifier circuit shown on Fig. 6 find expressions for the differential and common mode gains (v_3 / v_1 or v_4 / v_2) and common-mode rejection ratio (CMRR), assuming $R_1 = R_2$ and that the transistors are identical with $h_{oe} = h_{re} = 0$.

Calculate the CMRR if $R_5 = 10\ k\Omega$, $h_{ie} = 1\ k\Omega$, $h_{fe} = 200$, $R_1 = R_2 = 50\ \Omega$

Calculate the input impedance (between terminals 1 and 2) for differential signals.

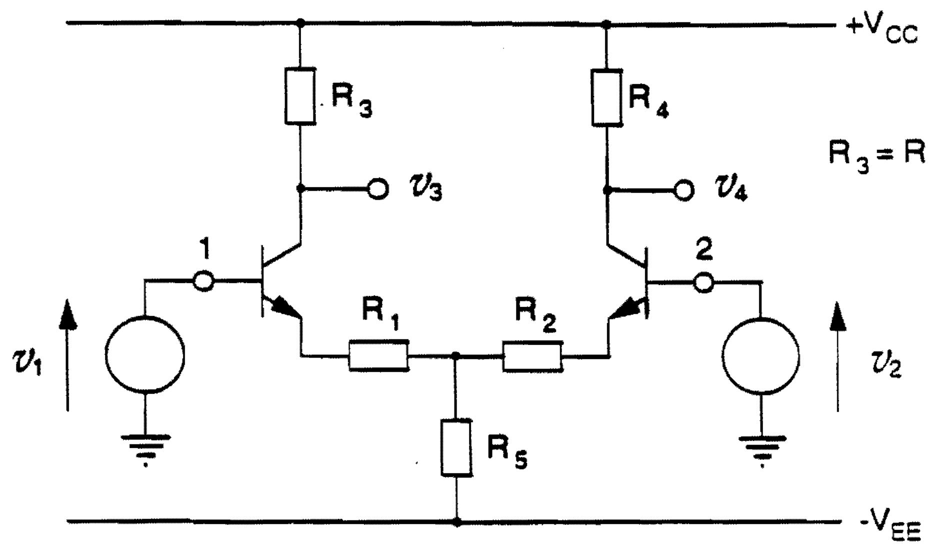

Fig. 6.

* 7. The circuit of Fig. 7 is designed to sink a constant current I through a load Z. Explain the physical action of the circuit. If the Zener diode holds the base of the transistor at 5 V and $R_4 = 1\ k\Omega$ what will be the current in the load ? Take V_{BE} for the transistor to be 0.7 V.

Find the small signal impedance looking into the collector of the transistor at terminal 2, not taking the load into account. The small signal parameters for the transistor are: $h_{ie} = 1\ k\Omega$, $h_{fe} = 200$ and $h_{oe} = 300\ \mu S$.

How could this type of circuit be incorporated into the circuit of Fig. 6 so as to improve its common-mode rejection ratio?

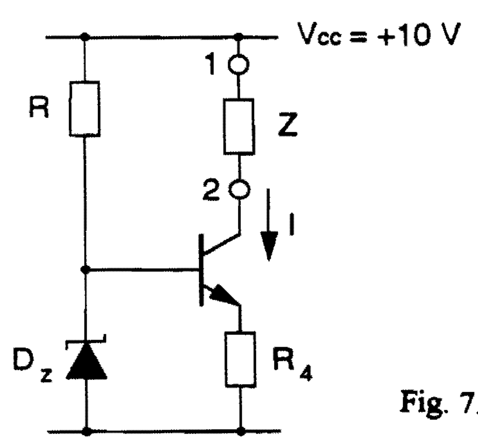

Fig. 7.

ANSWERS

1. i) 193 kΩ, 400 Ω, 398 Ω, 93 kΩ

   ii) in the range of (-70) to (-80)

2. i) -89, ~1 kΩ 357 Ω

   ii) ~508 Ω

4. -22; ~80 kHz

5. 13.5 – 24.0 V; 19.0 – 21.2 V; 13.7 kΩ, 2.76 kΩ

6. Differential gain = $-R_3h_{fe} / (h_{ie} + R_1(1 + h_{fe}))$

   Common mode again = $-R_3h_{fe} / (h_{ie} + (R_1 + 2R_5)(1 + h_{fe}))$

   CMRR = $(h_{ie} + (R_1 + 2R_5)(1 + h_{fe})) / (h_{ie} + R_1(1 + h_{fe}))$

   365, 22.1 kΩ

7. 4.3 mA; 0.33 MΩ

Suitable Tripos Questions

2004 IB Paper 5	Q1,Q2.
2003 IB Paper 5	Q1, Q2 parts (a) and (b)
2002 IB Paper 5	Q1
2001 IB paper 5	Q1, Q2
2000 IB Paper 5	Q1, Q2