Part 1A Paper 3: Electrical and Information Engineering,

EXAMPLES PAPER 2 Linear Circuits & Devices

This examples paper is based on material from lectures 5-9. Where possible, the lectures on which the questions are based are indicated, e.g. [L5]. As usual, questions containing material of tripos standard are marked *.

Electrical properties of materials, semiconductor diodes

1. Consider a solid slab of material as shown in Fig. 1. Calculate its electrical resistance assuming that it is made of (i) copper, (ii) silicon.

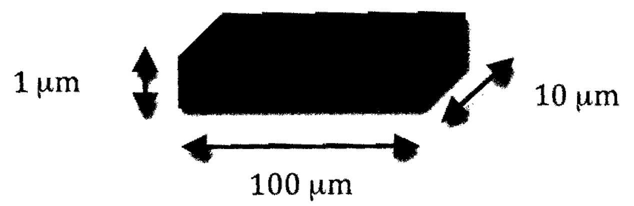


Fig. 1

If we assume that it has a dc voltage of 1V across its ends, calculate how much current will flow, and hence how much power will be dissipated in the slab, assuming it is made from copper. If in fact these slabs or wires were used as interconnects between the billion transistors in the latest microprocessor, how much power would they dissipate cumulatively, assuming they were made of copper? Discuss this qualitatively with your supervisor in terms of the continued increase in the number of transistors as each new microprocessor is developed. [L5]

2. A silicon diode with the I-V characteristics shown in Fig. 2 is used in the circuit below. Obviously the diode and the resistor have non-linear and linear characteristics, respectively, so we need to resort to a graphical method to determine the operating point of the diode. Find this operating point. Would you expect it to shift to the left or the right if the temperature were to increase by a few degrees, assuming the diode's characteristics depend more strongly with temperature than the resistor's? [L6]

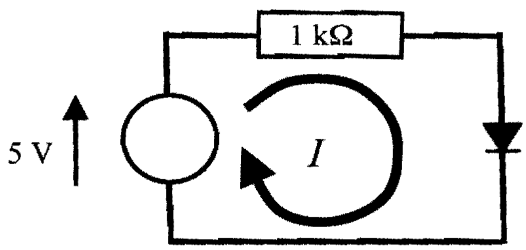
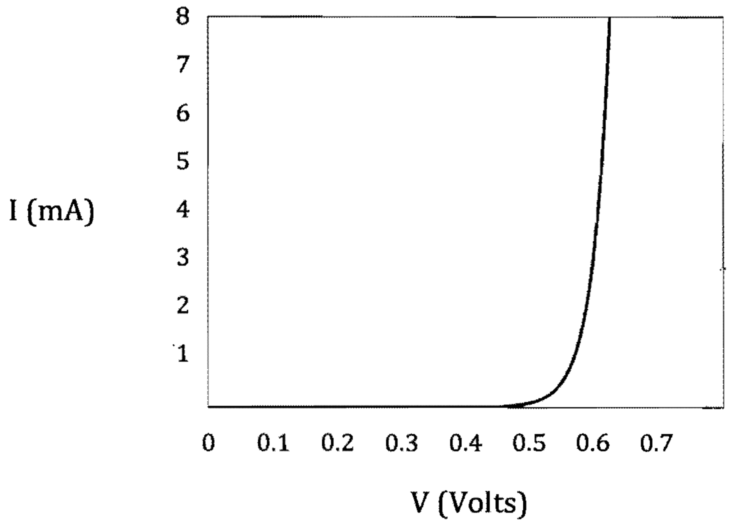


Fig. 2: diode I-V characteristics



3. Find the operating point of the diode in the circuit below in Fig. 3, assuming it has the same I-V characteristics as shown in Fig. 2. Also determine the output voltage, V_0. [L6]

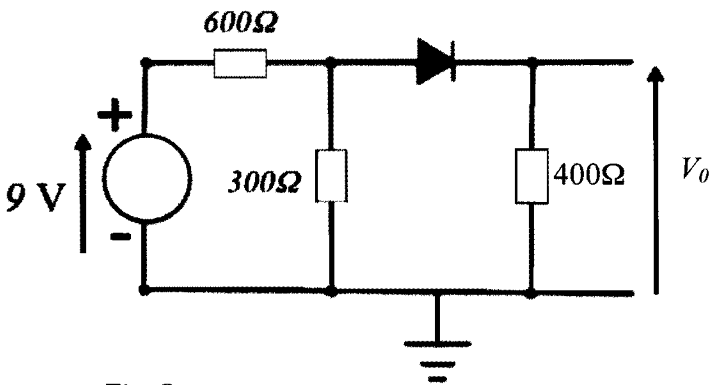


Fig. 3

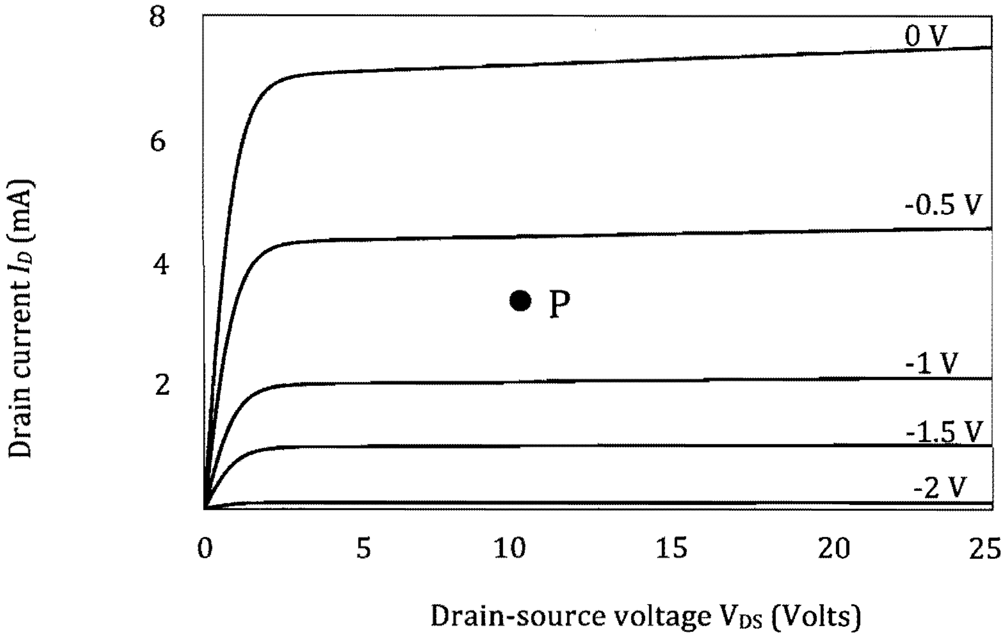
FET amplifiers

4. The characteristics and maximum ratings of a field-effect transistor (FET) are shown in Fig. 4.

(i) is the device a p-channel or n-channel FET?

(ii) Using the maximum ratings and the fact that you want to design an amplifier with as high an input resistance as possible and with an approximately linear relationship between input and output, eliminate the forbidden regions of operation of the FET. [L7]

Fig. 4 - FET characteristics



Absolute maximum ratings of FET:

Drain-gate voltage	25 V
Drain-source voltage	25 V
Continuous device dissipation	100 mW

5. A common-source amplifier circuit is shown in Fig. 5. The FET has the characteristics shown in Fig. 4.

(i) Calculate an appropriate value of R, and determine the bias voltage V_G required if the FET is to work at the operating point marked "P".

(ii) Graphically estimate the voltage gain for the case of a 0.5 V peak-to-peak voltage signal applied to the gate.

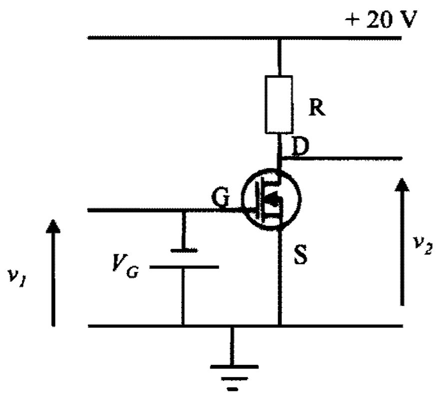


Fig. 5

6. The self-biased common-source amplifier circuit shown in Fig. 6 uses an FET with the same characteristics as shown in Fig. 4. Determine the values of the resistors R_1 & R_2 which will enable the transistor to be at the operating point, P. Discuss with your supervisor the advantages and disadvantages of having the resistor R_2 present.

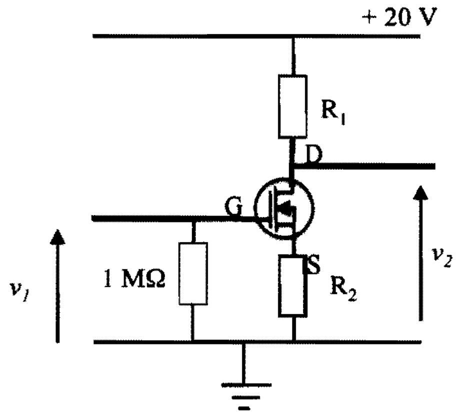


Fig. 6

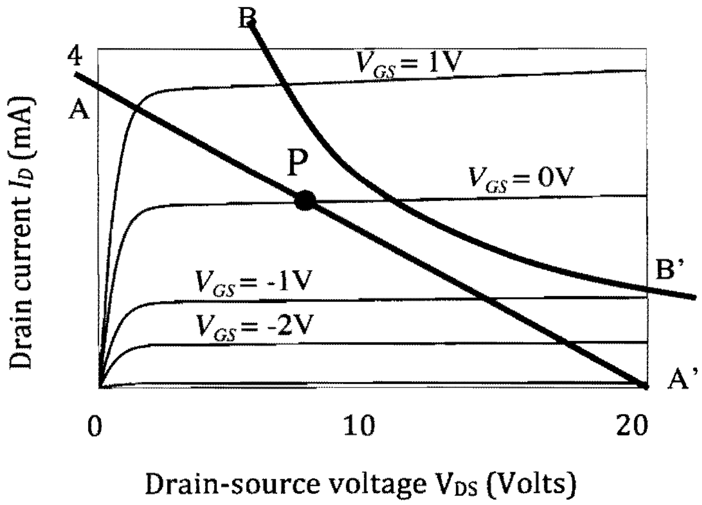
* 7. Figure 7 shows an amplifier circuit based on a FET, the *I-V* characteristics of which are also shown. We would like to implement the amplifier circuit shown, and for the circuit to have an input resistance of 1 MΩ, and the transistor to be at the operating point, P.

(i) What do the line A-A and the curve B-B represent?

(ii) A careless engineer proposes the following component values for the circuit: V_S = -20V, R_1 = 3.5 kΩ, R_2 = 1 MΩ. Show that these values are all incorrect, and determine what the correct ones should be.

(iii) For a small sinusoidal input signal v_i of peak value 1 V, graphically estimate the voltage gain of the circuit, assuming it has been implemented with the correct component values.

(iv) What is the purpose of the resistor R_1? Should it have a low or high value? Calculate the power dissipated in it when the input signal, v_i, is 1 V dc.



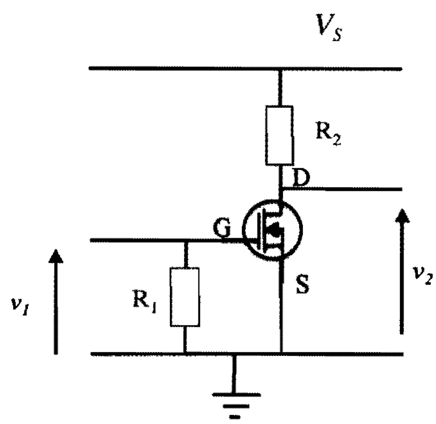


Fig. 7

Answers

1. 0.17Ω, $2.3\times10^{10}\Omega$, 5.88 W, 5.88×10^{9}W
2. 4.4 mA, 0.61 V. Shifts to the right.
3. $V_D = 0.61$ V, $I_D = 4$ mA, $V_0 \sim 1.6$ V
4. n-channel
5. (i) 2.86 kΩ, 0.75 V; (ii) ~ -15.4
6. 2.64 kΩ, 210 Ω
7. (i) A–A is the load line for a 5.68 kΩ load and + 20V supply, B-B is the max. power dissipation limit.

   (ii) + 20V, $R_1 = 1$ MΩ, $R_2 = 5.68$ kΩ.

   (iii) ~ -6.25

   (iv) Stops the gate floating if no input is connected. Use of a high value reduces the load on v_i. In this case the power drawn from the input is 1 μW.

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