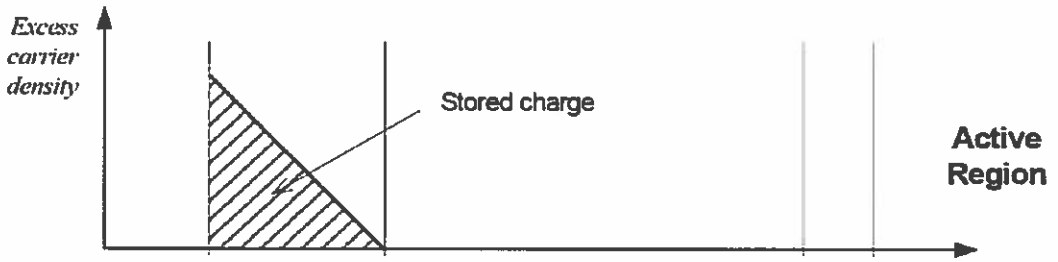
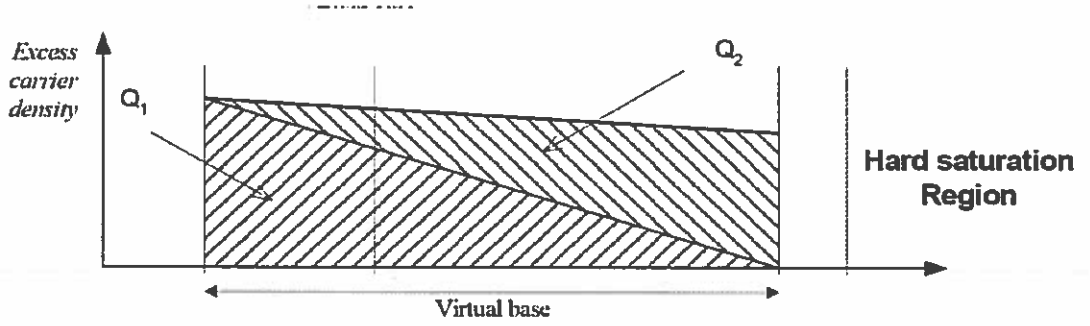
SOLUTIONS 4B2 2017

1. (a) linear region and saturation

Active region – BE junction forward biased, BC junction reverse biased. The charge is only stored in the base and the collector sees a high depletion region extending from the BC junction. No plasma is stored in the lowly doped collector region. This regime is good for amplification but not for switching as the voltage drop, V_{CE} is too high.



Deep saturation or 'hard saturation' region. Both BE and BC junctions are forward biased. The charge is stored in the base and the collector region. In deep saturation the plasma level is very high and the charge reaches the other side of the collector (where the n+ contact is). This regime is good for on-state but switching losses could be high as the deep plasma slows down the device during turn-off.



[25%]

(b) $f = \frac{1}{T} = 10\text{kHz} \Rightarrow T = 100\,\mu s$, $D = 50\%$,

$DT = t_{on} + t_r + t_d = 50\mu s \Rightarrow t_{on} = 50 - 0.5 - 1 = 48.5\mu s$

$(1-D)T = t_{off} + t_s + t_f = 50\mu s \Rightarrow t_{off} = 50 - 5 - 3 = 42\mu s$

ON -STATE

$$P_{ON} = \frac{1}{T}\int_0^{t_{ON}} V_{CE} I_C dt = V_{CE} I_C \frac{t_{on}}{T} = 2 \times 10 \times 0.485 = 9.7W$$

TURN – ON

$$P_d = \frac{1}{T}\int_0^{t_d} V_{dc} I_{OFF}\, dt = t_d f I_{OFF} V_{dc} = 3.75mW \text{ – (can be neglected)}$$

$$P_r = \frac{1}{T}\int_0^{t_r} I_C \frac{t}{t_r}[V_{dc} + (V_{CE} - V_{dc})\frac{t}{t_r}]dt = t_r f I_C [\frac{V_{dc}}{2} + \frac{V_{CE} - V_{dc}}{3}] = 4.23W$$

TURN – OFF

Delay time: $P_s = V_{CE} I_C t_s f = 1W$

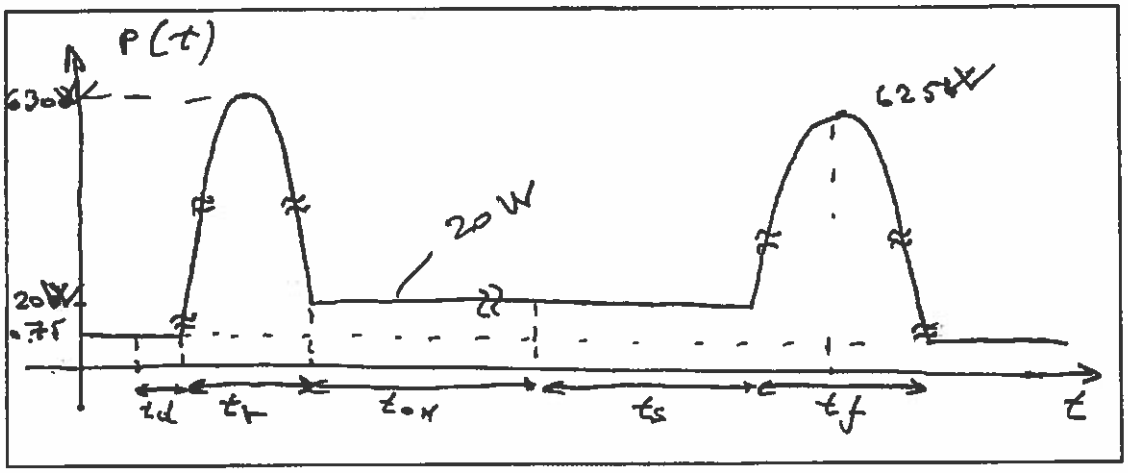
Current fall time:

$$P_f = \frac{1}{T}\int_0^{t_f} I_C (1 - \frac{t}{t_f}) V_{dc} \frac{t}{t_f} dt = t_f f I_C \frac{V_{dc}}{6} = 12.5W$$

OFF -STATE

$P_{OFF} = V_{dc} I_{OFF} t_{OFF} f = 0.031W$

Total losses (on-state + turn-on + turn-off): P total= 9.7+4.23+ 13.5+ 0.031= 27.46 W [40%]



[25%]

The power loss due to the base current can be calculated as:

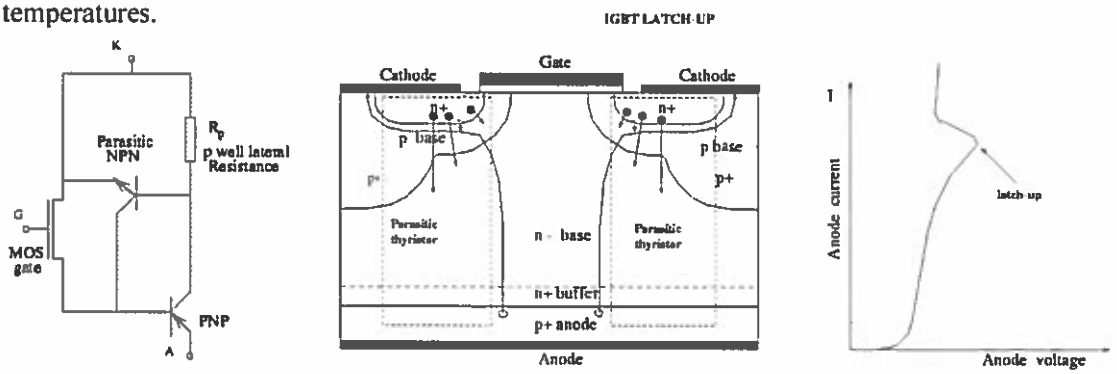
$$P_B = V_{BE} I_B D = 2.8W$$ [10%]

2. (a) The IGBT has a parasitic thyristor (n+ cathode, p well, n- base and p+ anode). To avoid the latch-up of this thyristor, the turn-on of the upper npn transistor must be suppressed. For that the lateral resistance of the p well should be kept as small as possible to avoid the turn-on of the emitter/base junction formed between the n+ cathode and the p base. This is accomplished by :

(a) introducing a deep p+ well diffusion short-circuited to the n+ cathode diffusion through a metal layer. The effect of this is to reduce the resistance of the p well lateral diffusion which lowers the voltage drop across the emitter/base junction

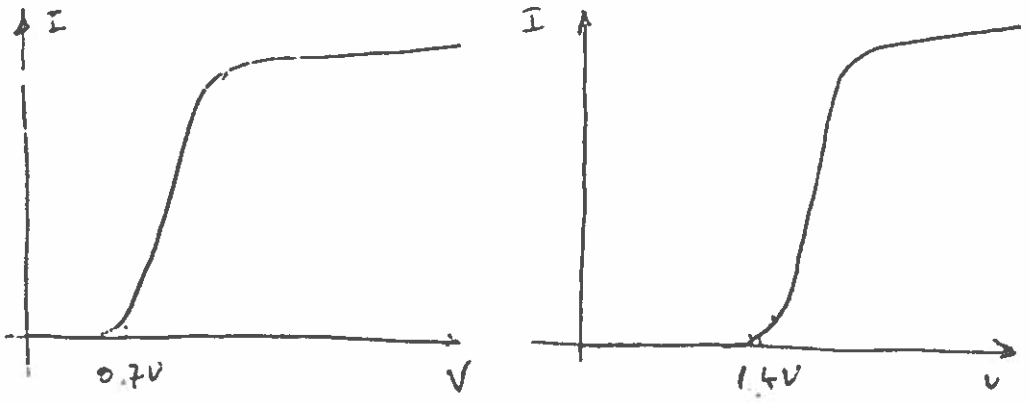
(b) reducing the length of the n+ (by for example using a trench gate structure which cuts the n+ diffusion).

(c) lowering the junction temperature (as the latch-up is exacerbated at higher temperatures) When the hole current under the n+ cathode develops a 0.7 V across the p well lateral resistance, the emitter junction of the npn transistor (i.e. cathode junction) becomes forward biased and the npn transistor turns on. This is followed by injection of electrons straight from the n+ cathode (which becomes an emitter) to the n- drift region (which acts as a collector). The npn together with the pnp will now form a thyristor feedback and the current can no longer be controlled by the gate. Moreover the IGBT in this conditions cannot be turned-off. The latch-up can also be prevented by lowering the lateral resistance of the pwell, lowering the gain of the pnp transistor, or lowering the operating junction temperature. This is because the npn transistor can be more easily turned on at higher temperatures.

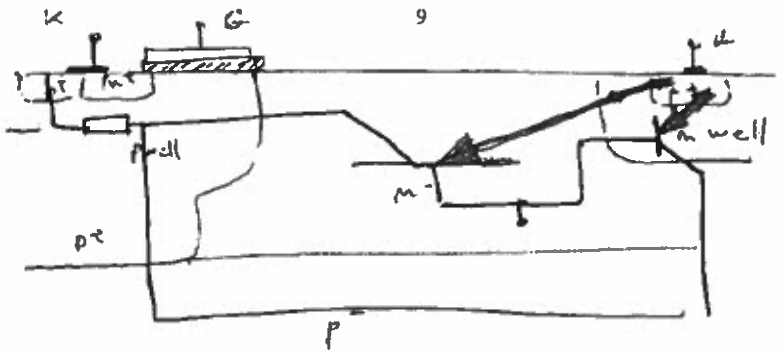


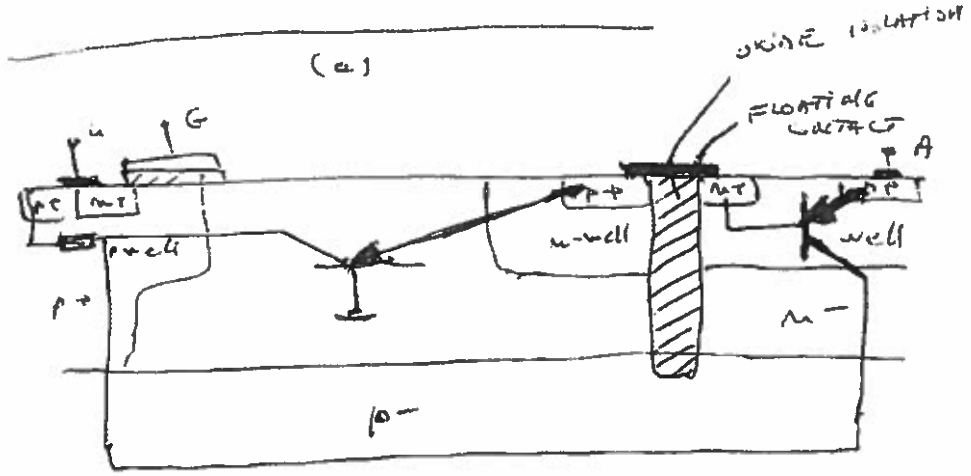
[30%]

(b) These are two LIGBT type structures. The structure (a) is based on two pnp transistors in parallel (one with wide collector and one with wide base). The MOSFET serves as the base current for both transistors. In general the wide collector (narrow base) transistor has a higher gain and could take more current than the wide base transistor. This structure is quite common in junction-isolation technology where the drift region plays the role of the wide base in one of the transistors and the p-substrate plays the role of the wide collector in the other transistor. The structure (b) is based on a electron MOS current driving the base of a Darlington pair of pnp transistors. The gain of the pnp transistor is slightly enhanced by the Darlington configuration but the effective base-emitter voltage is double compared to a single device. For this reason the on-state losses are quite high without offering any significant advantage. The I-V characteristics are shown below (not the differences in the shift voltage in the on-state)


I
0.7V
V
I
1.4V
v

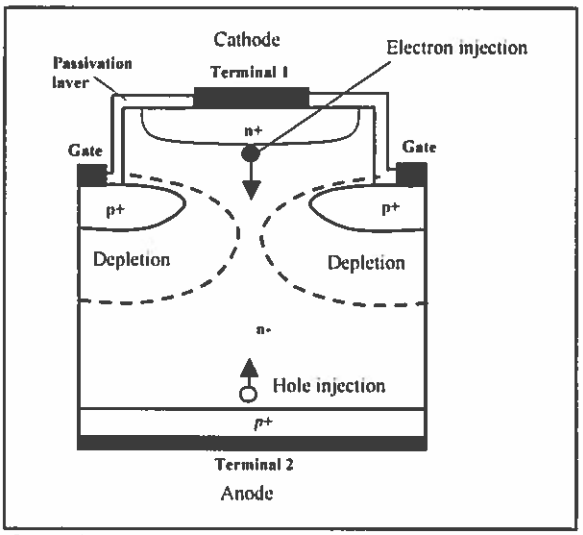
[35%]


K
G
S
n well
p well
p+
p-


(a)
OXIDE ISOLATION
FLOATING CONTACT
A
G
p well
n-well
well
p+
n-
p-

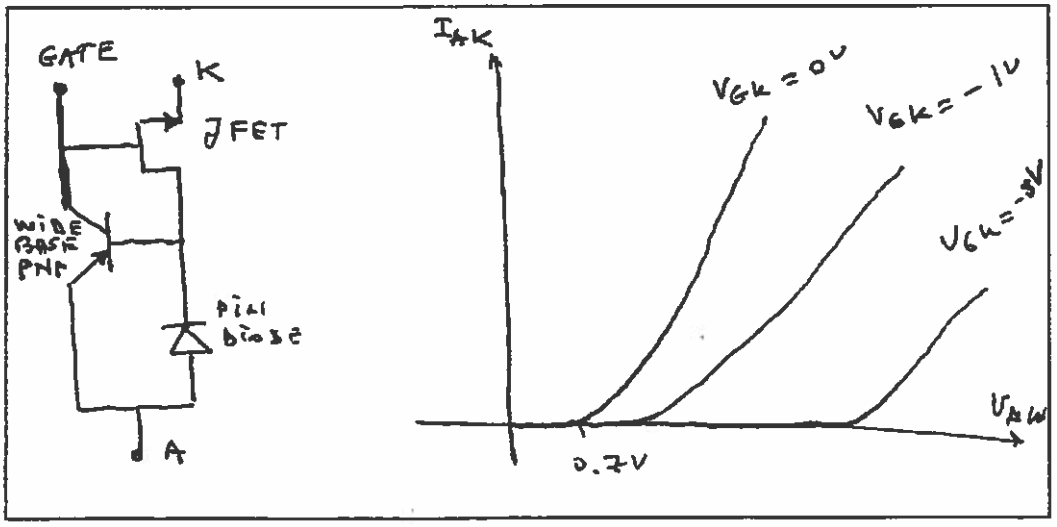
[35%]

3. (a) The structure is a variant of a Static Induction Thyristors (SIT). It is a junction controllable device and comprises a JFET, a diode and a PNP transistor. To obstruct the current flow and turn-off the device, the gate is biased negatively with respect to the cathode to form two depletion regions as shown in the next figure (this is similar to the way the JFET operates). When the two depletion regions meet, the current is pinched off, stopping the injection of electrons from the cathode. However, as opposed to a JFET, here we deal with a bipolar device as the p+ anode layer injects holes (similarly to a PIN diode or the emitter of a PNP transistor)



- In the off-state, during the blocking mode, when the anode (TERMINAL 2) is biased at high voltage with respect to the cathode (TERMINAL 1), the voltage is supported in the n- drift region. The p+ layers/n –drift junction is reverse biased and the two depletion regions formed from the p+ meet laterally to pinch the current.
- The device is turned on by removing the negative voltage applied to the gate connected to the p+ layers (or applying a slight positive voltage between the gate and the cathode). As result the depletion region around the p+ layers collapses allowing electron injection from the n+ cathode. This is followed by hole injection from the p+ anode and conductivity modulation.
- In the on-state, there are two bipolar structures which provide the conductivity modulation (and hence the plasma formation) in the drift region, the PIN diode formed between the p+ anode/n-drift and n+ cathode and the PNP transistor formed between the p+ anode as the emitter the n- drift as the base and the p+ gate as the collector. The plasma formation results in a lower resistance of the n-layer and superlinear I-V characteristics similar to those of a PIN diode.
- The turn-off of the device is achieved negatively biased the gate voltage with respect to the cathode potential. As a result, the depletion regions formed around the p+ layers pinch the electron current flow and consequently both the diode and the PNP transistor turn off. The plasma is removed by the depletion sweep of holes to the gate (and eventually a slow recombination process if no lifetime killing is present) [35%]

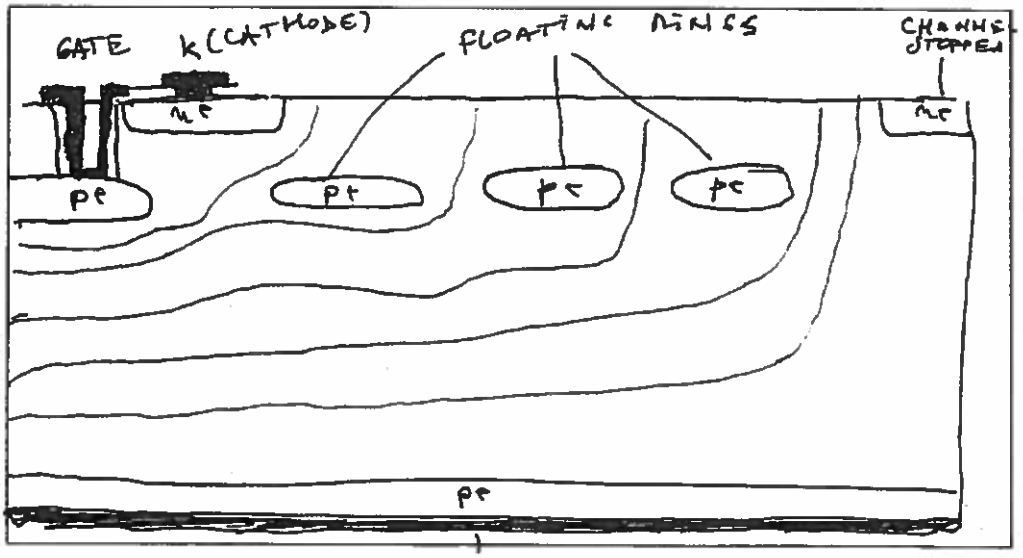
(b) The equivalent circuit and the I-V characteristics are shown below. The device comprises two active bipolar structures. A wide base pnp transistor connected between the anode and the gate and a PIN diode with the cathode connected to the collector of a JFET



[30%]

(c)

- Advantage: The device has very strong conductivity modulation as it has a double injection – similarly to that in a PIN diode and thyristor. As a result the on-state voltage drop could be smaller than in an equivalent IGBT.
- Disadvantages: The device has no high impedance control (MOS gate). The device also requires negative bias for keeping the device in the off-state, which means more complexity in the drive. [10%]



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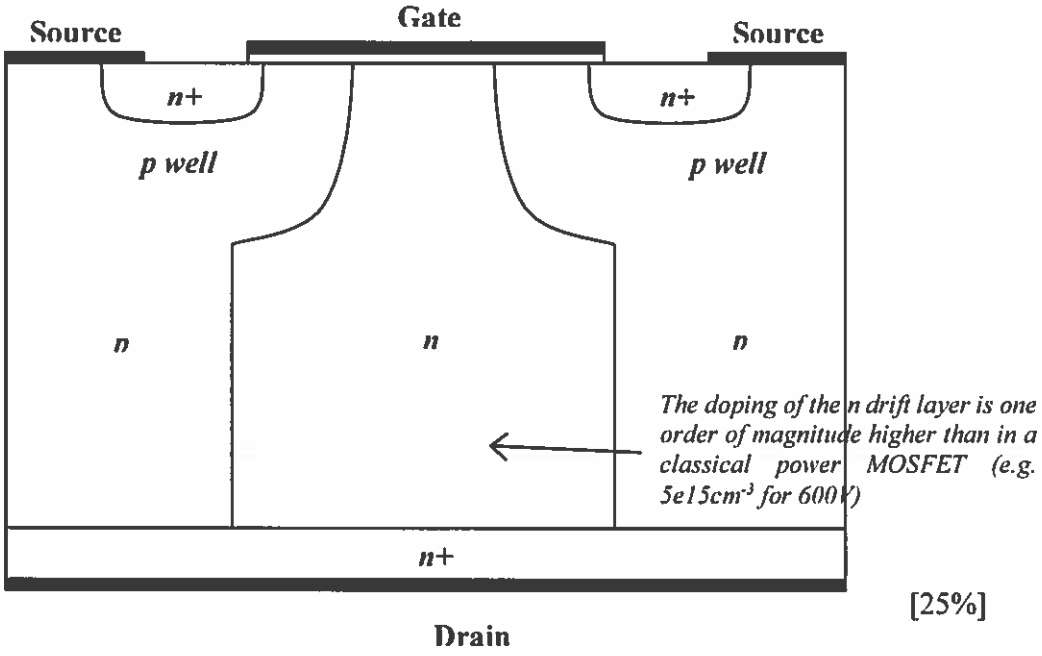
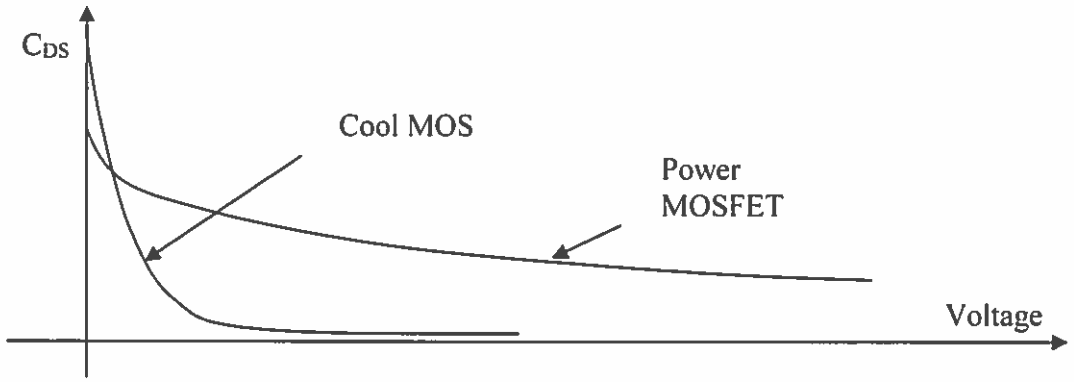
4. (a) (i) The Cool MOS is based the superjunction effect. The superjunction comprises multiple junctions disposed in the drift region with alternate layers of relatively highly doped n and p layers. The drift region is therefore made of thin and highly doped n/p stripes rather than a single n- layer. The depletion of the drift region is in this case dictated by these n/p multiple junctions rather than by the classical p+/n- junction. Since the stripes are very thin (compared to their length), they deplete at much lower voltage (due to the extension of the depletion region across the n/p junctions). The net advantage is a major reduction in the on-state resistance for the same breakdown capability. The electric field distribution is square rather than triangular, and the doping of the n pillars is considerably higher than that of the classical power MOSFET. For the same breakdown a reduction of 5-10 times in the on-resistance is possible.

The Cool MOS is shown below:



[25%]

(ii) The C_{DS} capacitance for the Cool MOS is high to start with, as the multiple junctions have a large (folded) area. At the same time the doping of the n and p pillars are very high limiting the extension of the depletion region at low voltages. These 2 effects lead to very high C_{DS} in Cool MOS at low voltages. At high voltages, in Cool MOS, the whole n-p pillar stack depletes, thus reducing sharply the capacitance. In contrast in Power MOSFET, the capacitance at low voltages is quite low (reduced area and reduced doping), while decreasing with $1/V^2$ at high voltages.



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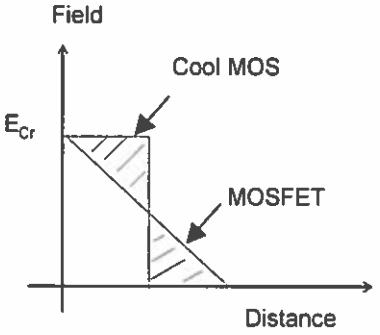
(b) (i) For MOSFET $w = w_{drift}$ (the depletion region at breakdown just reaches the n+ drain region)



$$V_{BQ} = \frac{E_{cr}}{2} W$$

$$V_{BR} = \frac{\varepsilon_0 \varepsilon_r E_{cr}^2}{2qN_D} \Rightarrow N_D = \frac{2qV_{BR}}{\varepsilon_0 \varepsilon_r E_{CR}^2}$$

drift length $w = \frac{2V_{BR}}{E_{CR}} \Rightarrow w_{drift} = w = \frac{\varepsilon_0 \varepsilon_r E_{CR}}{qN_D}$ - MOSFET

$w_{drift-CoolMOS} = \frac{w_{drift-MOSFET}}{2}$ (the drift width of CoolMOS is only half of that of MOSFET, as the field distribution for Cool MOS is rectangular rather than triangular – see picture above) [30%]

(ii) specific resistance for Cool MOS $= \frac{W_{CoolMOS}}{q\mu_n N_{D_{CoolMOS}}} \frac{X_n}{X_n + X_p}$

$N_{D\ Cool\ MOS} = 10\times N_{D\ MOSFET}$

$X_n = 1/2 X_p$ (to allow charge balance in the drift region of the Cool MOS)

$$\frac{R_{spcoolMOS}}{R_{spMOSFET}} = \frac{1}{10} \times 3 \times \frac{1}{2} = \frac{3}{20} = 0.15$$ [20%]