May 8, 2017 4B21 CRIB

Question 1

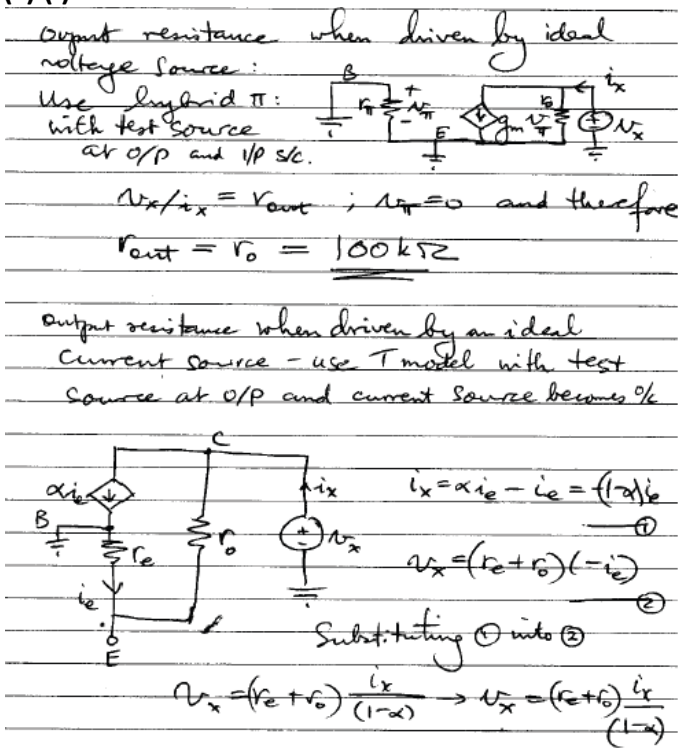
(a) Ideal voltage source is one where the voltage across it is independent of the current through it. Ideal current source is one where the current through it is independent of the voltage across it.

[10 marks]

(b) Hybrid-π and T-equivalent circuits are as shown below

[20 marks]

(c) (i)



$v_x/i_x = r_{out} = \frac{r_e + r_o}{(1-\alpha)}$

But $(1-\alpha) = \frac{1}{\beta+1}$

Therefore $r_{out} = (\beta+1)(r_e + r_o)$

and $(\beta+1) r_e = r_\pi$

So $r_{out} = r_\pi + (\beta+1) r_o$

$= 1k + (101)(100k)$

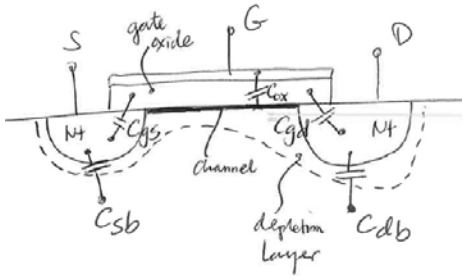
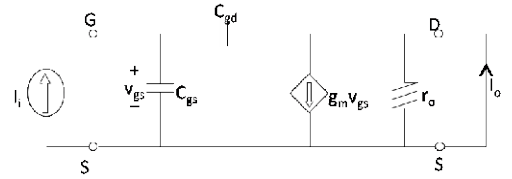
$= 10.1 M\Omega$

{50 marks)

(c) (ii) The common-base amplifier, when driven by low source resistance, behaves as a voltage amplifier. On the other hand, with high source resistance, it behaves like a current follower. This transition takes place when the source resistance is at the vicinity of the emitter resistance, r_e.

[20 marks]

4B21 Question 2

(a) **[25%]**	Gate-to-channel capacitance: linear region, Cgs = Cdg = (1/2) WLCox; Cox ~ 1fF/μm2 Gate-to-channel capacitance: saturation region, Cgs = (2/3) WLCox = Cdg =0 Overlap capacitance (~1-10 fF): Cgs = Cdg = WL_D where L_D = overlap length Source and drain junction capacitances C_{sb} and C_{db} (voltage-dependent) due to the depletion layer between S and D, and bulk (substrate) 
(b) **[20%]**	Equivalent circuit with the important C's. Here S is connected to the substrate (B) and C_{sb}, C_{db}, C_{gb} neglected to simplify analysis for unity gain frequency calculation  $i_o/i_{in} = g_m /[s(C_{gs} + C_{gd})]$ and current gain becomes unity when $\omega_T = g_m /[C_{gs} + C_{gd})]$
(c) (i) **[20%]**	The Miller approximation ssumes $v_o = -g_m R_L v_{gs}$ → we neglect the effect of C_L. This yields $f_H = 1/(2\pi C_{in} R_S)$ where $C_{in} = Cgs + Cgd\ (1+g_m R_L) = 20 + 5(1+1.25x10) =$ 87.5 pF. Thus f_H = 181.9 kHz
(c) (ii) **[15%]**	Gain = $-g_m R_L$ = -1.25 x 10 = -12.5 V/V Thus gain-bandwidth product is 12.5 x 181.9 MHz = 2.3 MHz
(c) (iii) **[20%]**	Gain can be reduced by reducing R_L through shunting the output with a lower load resistance. Alternatively the overdrive voltage (V_{GS}-V_T) can be increased by raising the bias current.

4B21 Question 3

Assume all transistors are matched.

(a) [10%]

A multistage amplifier has several circuit blocks connected in cascade; for example, the output of first stage becomes input of second stage and its output becomes input of the following stage and so on.

(b) [20%]

A multistage amplifier has many desirable circuit characteristics that a single stage does not. For example, it provides higher input-output isolation, higher input impedance, lower output impedance, higher gain, larger common-mode rejection, DC level-shifting, and possibly also higher bandwidth.

(c) (i) [40%]

Values of I_D, $|V_{OV}$, V_{GS}, g_m and r_o

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
I_D (µA)	45	45	45	45	90	90	90	90
V_{OV} (V)	0.15	0.15	0.3	0.3	0.15	0.3	0.15	0.15
V_{GS} (V)	-0.95	-0.95	1	1	-0.95	1	-0.95	-0.95
g_m (mA/V)	0.6	0.6	0.3	0.3	1.2	0.6	1.2	1.2
r_o (kΩ)	222	222	222	222	111	111	111	111

(c) (ii) [10%]

Voltage gain of 1st stage is $A_1 = -[g_{m1}(r_{o2}//r_{o4})] = -0.6\ (222//222) = -66.6$ V/V
Voltage gain of 2st stage is $A_2 = -[g_{m6}(r_{o6}//r_{o7})] = -0.6\ (111//111) = -33.3$ V/V
Thus the overall dc open-loop voltage gain = $A_1A_2 = 2218$ V/V**.**

(c) (iii) [10%]

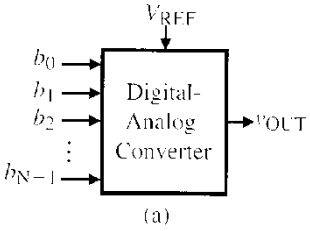
The lower limit of the input common-mode range is set by Q1 and Q2 leaving the saturation - occurs when the input voltage falls below the voltage at the drain of Q1 by |Vtp| volts. Since the drain of Q1 is at -2.5+1= -1.5V, then the lower limit is -2.3V.
The upper limit of the input common-mode range is set by Q5 leaving saturation. To remain in saturation, its V_{DS} should be at least equal to the overdrive V_{OV} i.e. 0.15V.Thus the highest voltage permitted at the drain of Q5 is 2.35V.
Thus the input common-mode range is 2.35-0.95 = 1.4V.

(c) (iv) [10%]

Highest allowable output voltage is when Q7 leaves saturation, i.e. $VDD–|V_{OV7}|= 2.5–0.15=2.35$V. Lowest allowable output voltage is when Q6 leaves saturation, i.e. $–V_{SS} + V_{OV6} = –2.5+0.3=–2.2$V. Thus the output voltage range is –2.2V to +2.35V.

4B21 Question 4

(a) The input to a DAC is a digital word consisting of parallel binary signals generated by a digital system. The corresponding output may take the form of a current or a voltage, but in either case is generated by scaling a reference.



DAC Block Diagram

A DAC with voltage output can be characterised by the block diagram shown. The voltage output V_{OUT} can be expressed as:

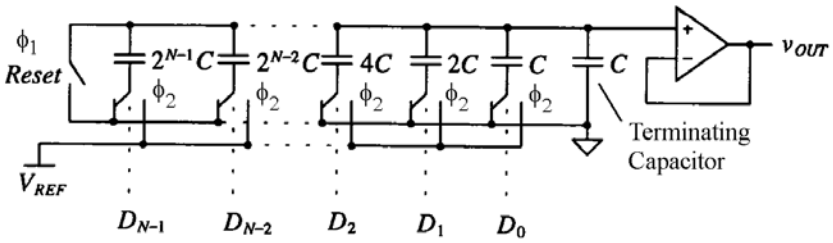
$$V_{OUT} = K_V V_{REF} D, \qquad \text{or} \qquad I_{OUT} = K_I V_{REF} D$$

where K_V and K_I are scaling factors, and D is a digital word given as:

$$D = \frac{b_0}{2^1} + \frac{b_1}{2^2} + \frac{b_2}{2^3} + \cdots + \frac{b_{N-1}}{2^N}$$

Charge-Scaling DACs

A popular implementation of DACs in CMOS technology is the charge-scaling approach. It is popular because of its structural simplicity and relatively good accuracy – resolutions in the 10 to 12-bit range can be achieved. The charge-scaling DAC operates by binarily dividing the total charge applied to a capacitor array, in effect implementing a digitally controlled voltage attenuator.



Charge Scaling DAC

Binary weighted capacitors

A parallel array of capacitors with binary-weighted values is used, as shown above, with one terminal of each connected to a unity-gain buffer amplifier with intrinsic very high input impedance. Each capacitor's second terminal is connected to one of a set of digitally-controlled electronic switches, each controlled by the state of a corresponding data bit (D_{N-1} to D_0). If the data bit is 0, the connection is to ground, and if it is 1, the connection is to a precise voltage reference V_{REF}. An additional terminating capacitor C is connected at the output of the array. The total capacitance is therefore $2^N C$, where C is a unit capacitance of a convenient value.

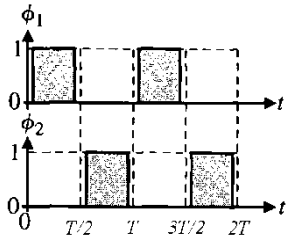
The resulting situation can be expressed by summing the charge in the V_{REF}-connected capacitors and evaluating the net potential when that charge is applied to the total capacitance $2^N C$. The ratio between v_{OUT} and V_{REF} due to the k-th capacitor may be written:

$$v_{OUT} = \frac{2^k C}{2^N C} \times V_{REF} = 2^{k-N} V_{REF},$$

it being assumed that the k-th bit, D_k, is 1, and all other bits are zero. Superposition then shows that the value of v_{OUT} for any digital input data word is:

$$v_{OUT} = \sum_{k=0}^{N-1} D_k 2^{k-N} \times V_{REF}$$ [40%]

(b) (i) **Reset switches**



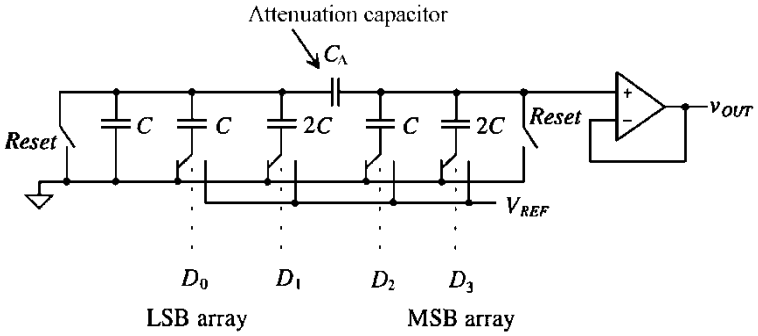
2-phase clock φ_1 and φ_2

A two-phase non-overlapping clock φ is required to control the state of the switches.

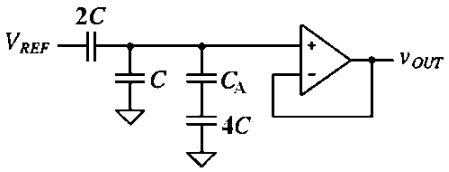
Its characteristics are shown in here. It can be seen that two distinct phases are defined, according to which of the signals φ_1 and φ_2 is active (normally taken as logic 1).

Consider the initial condition, which is the interval when φ_1 is active. The top and bottom plates of all capacitors in the array are grounded, and all capacitors discharged. When φ_2 is active (and by definition φ_1 is inactive), those capacitors connected to switches whose data inputs are 1 become charged to V_{REF}, while those with control inputs set to 0 remain uncharged. [10%]

(ii) **Problem section**



With D3 set to 1 and all other bits set to zero, the resultant equivalent circuit is shown below. The circuit can be considered as a voltage divider.



The expression for the voltage at the input to the unity-gain buffer (also v_{OUT}) is:

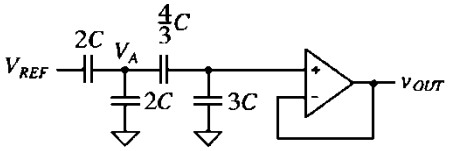
$$v_{OUT} = \frac{2C}{(C_A \text{ series with } 4C) + C + 2C} \times V_{REF}$$

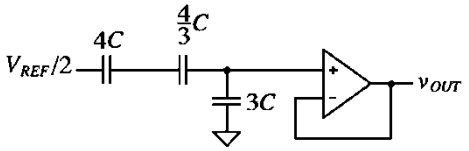
$$= \frac{1}{2} V_{REF}$$

Cancelling C and V_{REF}, and solving, $C_A = \frac{4C}{3}$

This value holds good for a 4-bit converter. A different value for C_A is needed for converters of other resolutions implemented using the split-array architecture. [20%]

(iii) If D1 = 1 and all other inputs are 0, the new equivalent circuit is as shown below left, with the attenuation capacitor shown, $C_A = \frac{4C}{3}$.





This equivalent circuit can be further simplified using a Thevenin approach to the circuit below, which can be evaluated more simply as a charge-scaled divider. The voltage at the buffer input (and hence v_{OUT}) is:

$$v_{OUT} = \frac{(4C \text{ in series with } 4C/3)}{(4C \text{ in series with } 4C/3) + 3C} \times \frac{V_{REF}}{2}$$

4C in series with 4C/3 is $\frac{4 \times 4/3}{4+4/3} C = C$; hence

$v_{OUT} = \frac{C}{C+3C} \times \frac{V_{REF}}{2} = \frac{V_{REF}}{8}$ (as expected).

[10%]

(iv) **Advantages of split-array**

As the number of bits increases, the ratio of the MSB capacitor to the LSB capacitor becomes large. For example, if the unit capacitor C were chosen to be 0.5 pF and a 16-bit DAC was to be designed, the MSB capacitor would need to be:

$$C_{MSB} = 2^{N-1} \times 0.5 \text{ pF} \quad = \quad 16.384 \text{ nF}$$

This is a large value, difficult to realise on-chip. In a typical process with layer-to-layer capacitance of 0.5 fF/μm^2, the area required would be approximately 3×10^7 μm^2, or over 5mm square. The total capacitance needed would in fact be almost twice this when all capacitors are taken into account.

It is possible to reduce total capacitance required by splitting the array into two (or more) parts. In the example given, a 4-bit converter is achieved using two 2-bit sub-arrays, one handling the 2 MS bits, the other the 2 LS bits. The largest capacitor needed is 2C. In a non-split design, the largest would be 4C. This advantage also applies to higher resolution converters with more bits, where a substantial reduction in total C (and hence chip area) can be obtained. [10%]

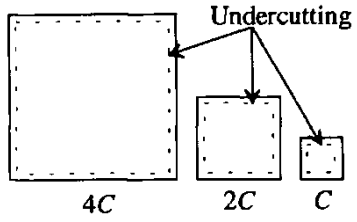
(v) **Precision**

The precision achieved depends on the accuracy with which the capacitors can be defined.

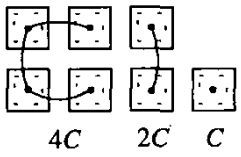
For example, the diagram below shows a 3-bit binary capacitor array using three capacitors, *C*, 2*C* and 4*C*. When the capacitors are fabricated, undercutting of the mask will affect each to a different extent dependent

on its perimeter, and will cause an error in the ratio of the capacitor values, potentially leading to errors in linearity as N increases.

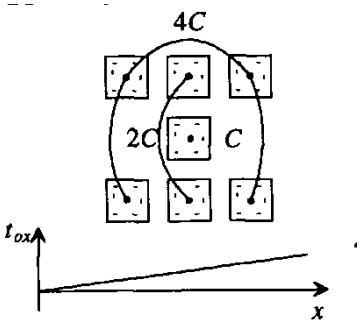
A simple solution is the use of unit capacitors of identical dimensions wired together in groups of 2, 4, 8 … etc. Undercutting then affects all capacitors identically, and the ratios between capacitors are maintained.



(a) Layout of a binary-weighted capacitor array using individual capacitors. Undercutting affects each differently.



(b) Using unit capacitors to minimise effects of undercutting.

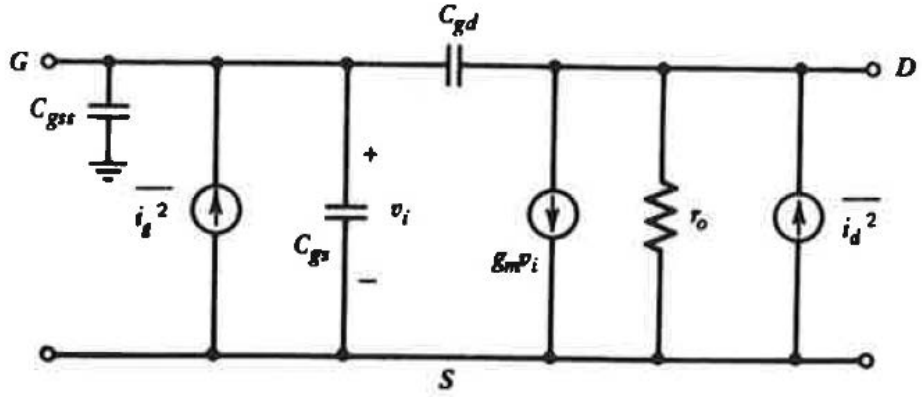
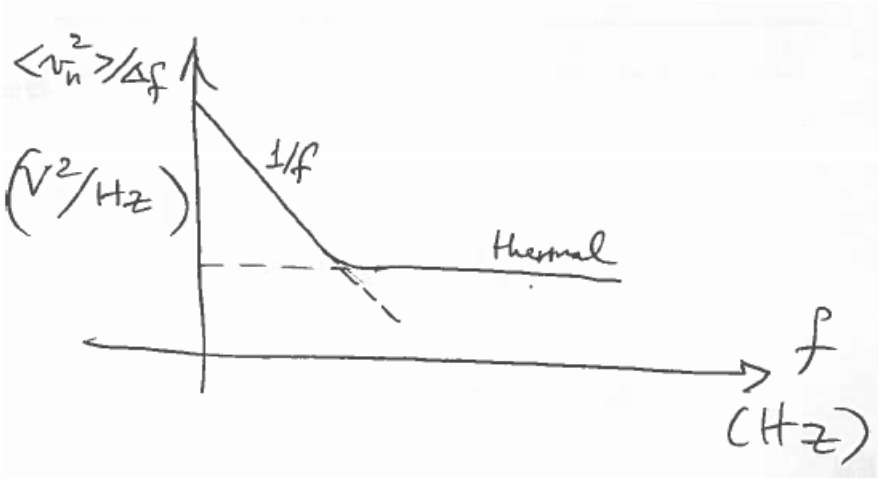


(c) Using common-centroid layout to minimise variations due to oxide thickness gradients.

Even if this approach is taken, non-uniformities in the oxide thickness may lead to a gradual variation in the specific capacitance of the dielectric with position (referred to as gradient errors). This can be combatted by the use of a common-centroid layout scheme, with the various capacitors similarly disposed around a common centre point. To first order, errors due to gradual variation in oxide thickness average out to be the same for each capacitor.

A further limitation of this architecture arises because of the existence of a parasitic capacitance, which may be significant, at the input of the buffer amplifier. This limits its use as a high-resolution data converter. [10%]

4B21 Question 5

(a) **[20%]**	Given are five types of noise in integrated circuit components – any three would be acceptable. -- Flicker (or $1/f$) noise – dominates at low frequency. -- Thermal noise, shot noise – this noise is also referred to as "white" noise since it is present at all frequencies (flat spectrum) -- G-R noise – has a $1/f^2$ spectrum -- Popcorn (or burst) noise – at low frequencies.
(b) **[20%]**	 $< i_g^2 > = 2\, q\, I_G\, \Delta f$ $< i_d^2 > = 4\, k\, T \left(\frac{2\, g_m}{3}\right) \Delta f + K \frac{{I_D}^a}{f}\, \Delta f$ 

(c) **[30%]**	Assume no gate current noise (since its connected to a low impedance signal source) and operation at high enough frequencies so that flicker noise is negligible. Output noise voltage $<v_o^2>/\Delta f = 4kT\,(2g_m/3)\,R_L^2 = (4kT/q)\,(2g_m/3)qR_L^2$. With g_m = 1.25 mA/V^2 and R_L =100 kΩ , $<v_o^2>/\Delta f = 0.133\text{x}10^{-12}$ V^2/Hz and $(<v_o^2>/\Delta f)^{1/2} = 0.365\text{x}10^{-6}$V/√Hz. Hence EIN = $(<v_o^2>/\Delta f)^{1/2}/A_V$ = 0.365uV/√Hz/200 = 1.8 nV/√Hz.
(d) **[10%]**	Noise Figure is a figure of merit characterizing how noisy an amplifier is with respect to an ideal (noiseless) amplifier. $NF = 20 - 20log\frac{S_{vo}}{N_{vo}}$ (the 20 comes from $S_{vi} = 10N_{vi}$) S_{vo}, N_{vo} are from measurements.
(e) **[20%]**	The first amplifier should have the lowest noise figure to obtain the lowest overall noise figure. Gains of A, B, C are 4, 16 and 100, respectively. Thus A should be the lowest in the cascade. For the 2nd amp in the cascade, the choice is between B or C. If we choose the order A, B, C then the overall noise figure is $NF = NF_A + (NF_B-1)/G_A + (NF_C-1)/G_AG_B$ = 1.997. If we choose A, C, B, then the overall noise figure along similar lines is 2.475. Hence the order A, B, C yields the lowest overall NF.

END OF PAPER