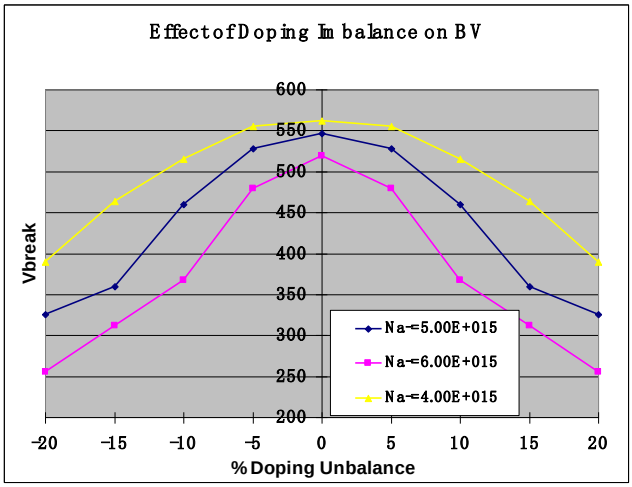
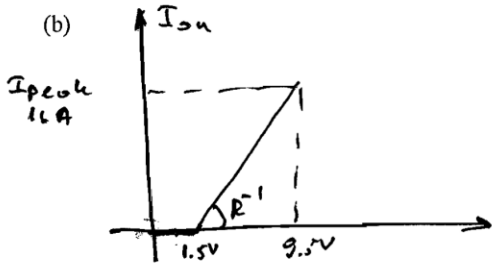
Answers 4B2 - 2018

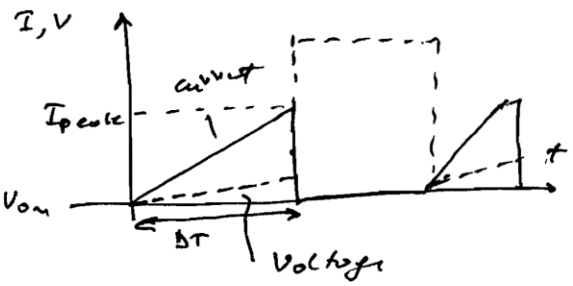
(a) The voltage blocking in a classical MOSFET is based on the extension of the depletion voltage at the p-well/n drift junction when the drain voltage is increased. To accommodate a large voltage to be supported by this region, the doping of the drift region must be low and the drift region must be thick. In a Superjunction MOFSET, p and n pillars are placed within the drift region. The depletion region forms at the interface between the n and p pillars and the pillars must deplete at much lower voltage than the breakdown voltage of the device. The charge balance ensures that both the n and p pillars are depleted. If for example the n pillar has more donor charge than the acceptor charge in the p pillar, the p pillar depletes but the n-pillar depletes at much higher voltages resulting in earlier breakdown at the top of n and p pillars next to the p well. The graph below shows a simulation of the breakdown voltage function of the doping imbalance (as a percentage of charge) for 3 different charge levels in the n-pillar. It clearly shows that any imbalance in the charge between n and p pillars results in a deterioration of the breakdown.



[30%]

(b)





$$P_{on} = \frac{1}{T}\int_0^{\Delta T} VI\,dt = \frac{1}{T}\int_0^{\Delta T} \alpha \cdot t\,[V_{offset} + R\alpha t]\,dt$$

where α is the ramp of the current growth in time

$$\alpha = \frac{I_{peak}}{\Delta T}$$

$$P_{on} = \int_0^{\Delta T} \frac{I_{peak}}{\Delta T} V_{offset}\, t\,dt + \int_0^{\Delta T} \left(\frac{I_{peak}}{\Delta T}\right)^2 \cdot R\, t^2\,dt$$

$$= \frac{I_{peak} \cdot V_{offset}}{2}\Delta + \frac{I_{peak}^2 R}{3}\Delta =$$

$$= \frac{16 \cdot 1.5}{2}\cdot\frac{1}{2} + \frac{16^2 \cdot \frac{1}{2}}{3}\cdot\frac{1}{2} = \underline{\underline{27.33\ W}}$$

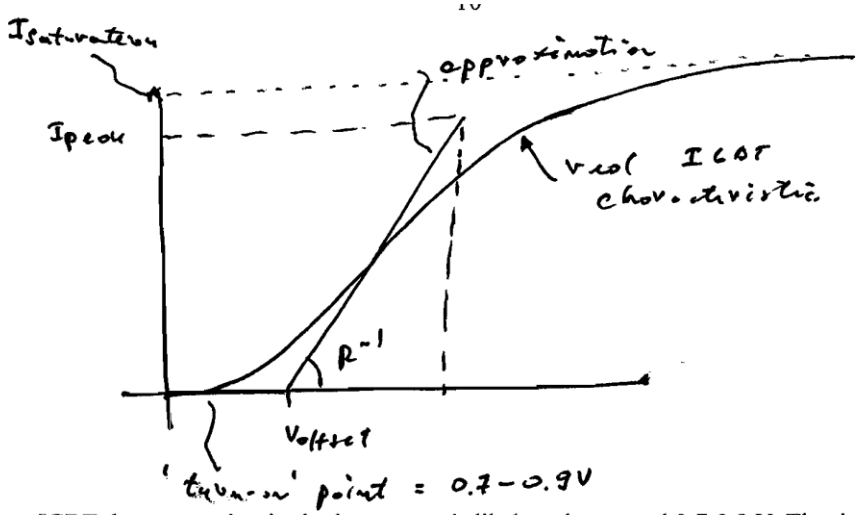
[3%]

$P_{turn-off} = E \cdot f = 3 \cdot 10^{-3} \cdot 50 \cdot 10^3 = 150\ W$

The switching losses are much higher than the on-state losses indicating that the switching frequency is too high.

f should be around $\underline{\underline{10\ kHz}}$ for a more balanced system

[20%]



In an IGBT the turn-on' point in the on-state is likely to be around 0.7-0.9 V. That is ssmaller than Voffset which is 1.5 V. So at low currents, the approximation is likely to overestimate the voltage drop on the IGBT. The approximation is based on a linear increase in the current with the voltage beyond the offset voltage. In reality, as the device heads towards the saturation, the characteristics become sub-linear and the approximations is likely to underestimate the voltage drop on the IGBT. We also make the assumpations that the peak current Ipeak is greter than the saturation current.

So if the SMPS peak on-state current is much lower, when compared to the saturation current of the IGBT, it is most likely that the approximation will overestimate the on-state voltage drop in the IGBT. A practical device would therefore have lower on-state losses than those predicted by using eq. 1.

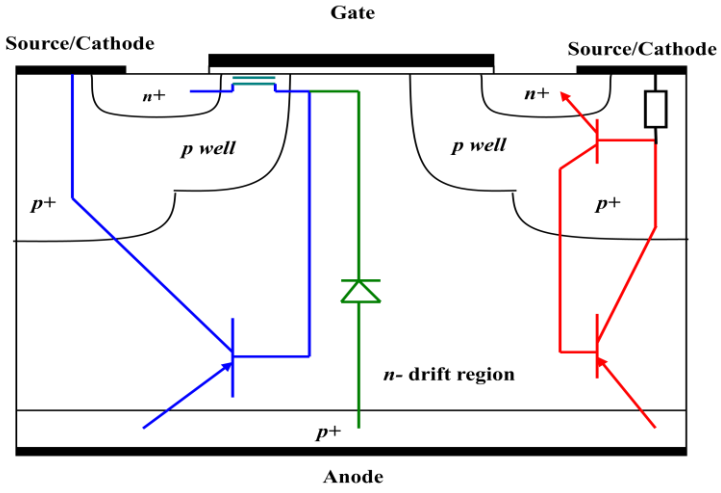
On the opposite, if the peak current is close to the saturation current of the IGBT the approximation will underestimate the on-state voltage drop in the IGBT. A practical device would therefore have much higher on-state losses than those predicted by using eq. 1. [2 0/3]

2. (a) The IGBT has within its structure three MOS- bipolar devices:

(i) The cascade MOSFET - PIN diode - responsible for double side plasma injection – electrons from the accumulation layer and holes from the p+ anode layer. This leads to conductivity modulation of the drift region.

(ii) MOS base current controlled - wide base PNP transistor - responsible for single side hole injection from the p+ anode which leads to conductivity modulation of the drift region.

(iii) Parasitic MOS turn-on thyristor - must be always suppressed as this would lead to latchup and malfunction of the device.



[30%]

(b) (i) **Over current Sensing and Protection.** The sense IGBT has an identical structure to the main IGBT, but a fraction of the active area. The Sense IGBT takes a known fraction of the current (say 100x less) of the main IGBT. By measuring the current in the Sense IGBT, the current in the IGBT could be calculated. The current in the Sense IGBT (and hence in the main IGBT) is measured by the voltage drop on the resistor R1 (sensing) When the voltage drop on R1 exceeds the threshold voltage of the MOSFET M1 , then M1 is turned off and pulls down the gate of the main IGBT, thus lowering the current on the IGBT (protection function).

Over voltage sensing and protection. The avalanche diode DAval becomes active during the blocking mode. DAval is designed to break down just before the IGBT breaks down. When the avalanche diode breaks down the gate of the IGBT is pulled up, thus turning on the main IGBT. The avalanche current is then spread over a large area (rather than being concentrated in a spot), thus allowing higher avalanche current to be supported during the breakdown. The idea is to avoid thermal failure due to localised avalanche.

Over temperature sensing and protection

Ds1 to Sn are thermal diodes. They are operated in forward bias and biased with a constant current supplied by the current mirror made with M3, M$ and Rref. Rref adjusts the current level. The voltage drop in each of the thermal diodes, decreases lineally with temperature with approx. -2mv/C. The diodes are put in series to increase the total voltage drop across them. When the temperature in the device reaches a certain level (designed to be equal or less than the junction temperature) – say 175C, the voltage drop on the series D11 and Dsn reduces thus pulling up the gate of M2. If M2 turns on the gate on the main IGBT is pulled down, thus reducing the current in the main IGBT and hence lowering the temperature.

RG adjusts the delay in the turn-off and modulates the dV/dt. D1 prevents the forward bias of DAval.

[50%]

(c) The Sense IGBT should have an identical structure and design to the main IGBT, except that has much smaller active area (say 100X smaller). There are two possible issues concerning the scaling of the current in the Sense IGBT compared to the Main IGBT: (i) Because of the voltage R1, both the Vds and the effective Vgs in the sense IGBT are smaller than in the main IGBT. Thus the scaling of the current is not perfect. The Sense IGBT will enter saturation earlier than the main IGBT. (ii) the temperature in the sense IGBT could be different than in the main IGBT – because of (i) but also because of different placement within the smart chip. [20%]

3. (a) The structure is a variant of a Static Induction Thyristor (SIT). It is a junction controllable device and comprises a JFET and a main thyristor. Terminal 1 is the Cathode, Terminal 3 Anode and Terminal 2 is the control terminal (gate). An additional thyristor formed between TERMINAL 2 and TERMINAL 1 is present. To obstruct the current flow and turn-off the device, the gate is biased negatively with respect to the cathode to form two depletion regions (this is similar to the way the JFET operates). When the two depletion regions meet, the current is pinched off, stopping the

injection of electrons from the cathode. However, as opposed to a JFET, here we deal with a bipolar device (a thyristor) as the p+ anode layer injects holes while the n+ injects electrons.

- In the off-state, during the blocking mode, when the anode (TERMINAL 3) is biased at high voltage with respect to the cathode (TERMINAL 1), the voltage is supported in the n- drift region. The p+ layers/n –drift junction is reverse biased and the two depletion regions formed from the p+ meet laterally to pinch the current. The p-well/n- drift region is also reverse biased just as it is in classical thyristor.

- The device is turned on by removing the negative voltage applied to the gate (TERMINAL 2) connected to the p+ layers and subsequently applying a positive voltage between the gate and the cathode. As result the top pnpn thyristor formed between TEERMNAL 2 and TERMINAL 1 turns on supplying holes to the p well. This is followed by the triggering of the main thyristor when the TRERMANL 3 is at a positive voltage
- In the on-state the n- drift region is heavily modulated by the plasma supplied by the main thyristor.
- The turn-off of the device is achieved negatively biased the gate voltage (TERMOINAL 2) with respect to the cathode potential. As a result, the depletion regions formed around the p+ layers pinch the electron current flow and consequently cuts the thyristor path. The plasma is removed by the depletion sweep of holes to the gate (and eventually a slow recombination process if no lifetime killing is present). This is however the weak point of this structure, as the thyristor action is very difficult to break using a JFET effect. This requires that the two terminal 2 layers are very close to each other.

[60%]

(b) - Advantage: modulation using double side injection of plasma (electrons from the Terminal 1, and holes from Terminal 3). This means better on-state performance and lower voltage drop in the on-state.

- Disadvantage 1: Slow and difficult to turn-off than a JFET which is a unipolar device. Th depletion region enabled by the JFET action is much less effective when plasma is present in the device.

- Disadvantage 2: Difficult to manufacture as involves several additional layer.

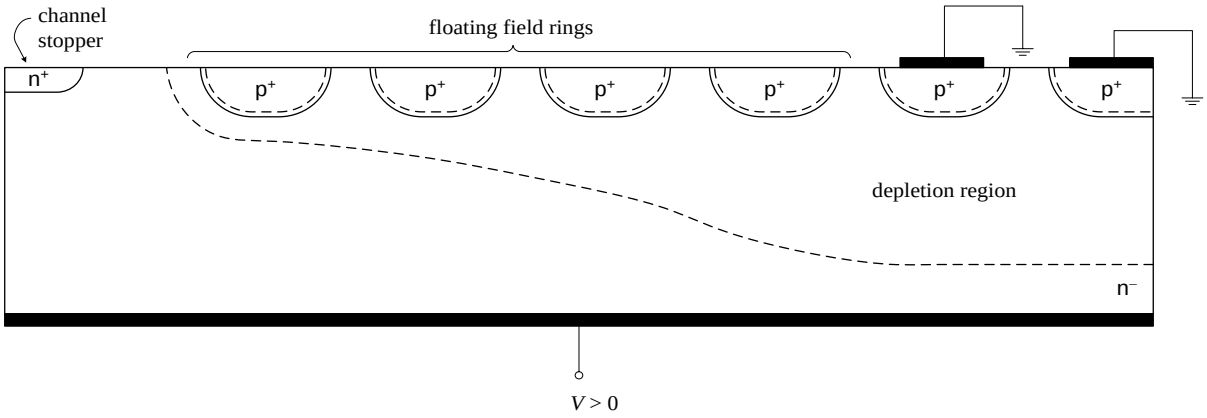
- Disadvantage 3 – The turn-on of the top pnpn thyristor formed between TERMINAL 2 and TERMINAL 1 requires current and pulse control. This means that the driving circuit is very complex. [20%]

(c) The p –well is changed to an n-well – this becomes a static induction thyristor where instead of a classical thyristors, a PIN high voltage junction is present. The terminal 2 still acts as a gate modulation the current path through the PIN diode. [20%]

4. (a) The shape of the junction which supports the voltage plays an important role in ‘field crowding’. The higher the radius of a cylindrical or spherical junction the closer the breakdown is to that of an ideal parallel-plane junction. However, in most microelectronics processes the junction depth is limited to a couple of microns up to maximum 10-15 microns. The curvature effect can be reduced in multiple cell power devices such as MOSFETs or IGBTs by placing the cells (with multiple junctions) close together to simulate almost a ‘continuous junction’. Field plates can also be used to reduce the curvature effect.

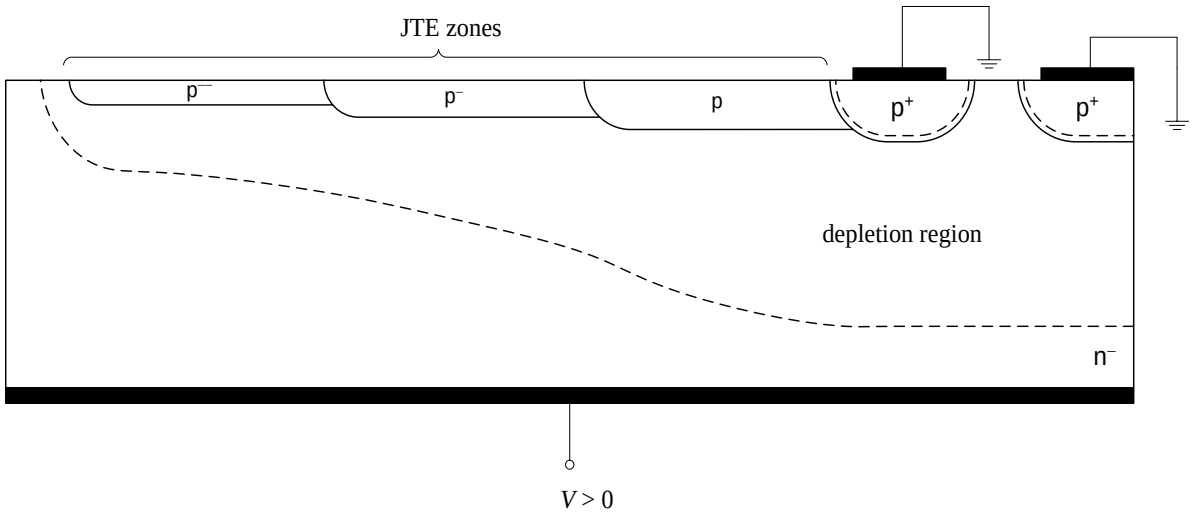
Floating Rings

The use of multiple floating rings (concentric highly doped p+ rings surrounding the active area of the device). The idea is to gradually release the depletion region at the edge of the device. The voltage is supported between each pair of p+ rings thus reducing the crowding of the electric field at the surface. The spacing and depth of the rings are designed such that the electric field peaks at the surface between each pair of rings are almost equal and the breakdown voltage of the final structure is at least 90% of the bulk breakdown.



Junction Termination Extension (JTE)

Use of multiple zones with the doping level decreasing from the active area towards the end of the termination. The effect is similar to that achieved by the field rings – that is the gradual release of the depletion region at the edge of the device. The voltage is ideally supported uniformly along the JTE zones.

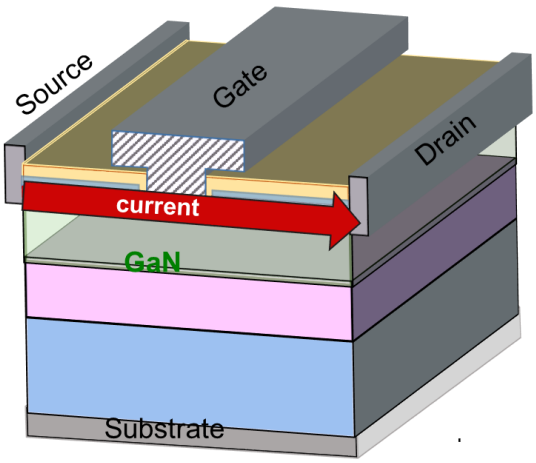


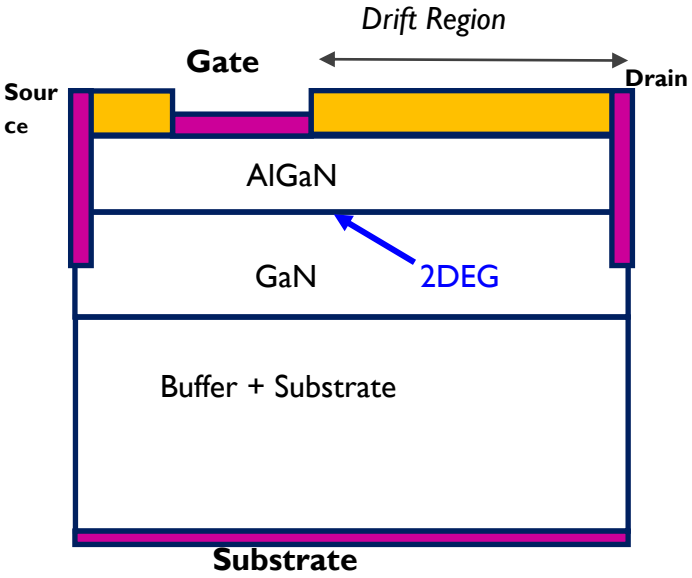
[40%]

(b) The field rings that are closer to the active area have a smaller equivalent radius of a spherical (or cylindrical) junction when compared to the field rings that are farther away from the active area. Therefore to avoid high electric fields next to the active area, the inner rings should have a smaller distance between them. Hence they absorb a smaller voltage between them compared to the outer rings. A good optimisation is when all the electric field peaks between the rings are equal at breakdown so the device theoretically breaks in all points at the same time. This would lead to the maximum efficiency of breakdown per unit area. For this the distance between the rings should be increased gradually from the first ring (i.e. the ring that is the closest to the active cell) to the last ring (the farthest from the active cell). [20%]

(c)

HEMT structure





The device is based on a two dimensional Electron gas (2DEG) formed between a GaN buffer and an AlGaN layer placed on top. The current flows from the source to the dran through the 2DEG layer. The gate modulates the flow and can turn-on or turn-off the device. Increasing the gate to drain distance allows higher breakdown, as this relaxes the electric field between the gate and drain but results in higher on-state resistance. [20%]

(d) Advantage1 : GaN is wide bandgap material which offers much higher critical electric field than silicon. Hence the dimensions of a HEMT are much smaller for the same rated voltage. This results in much lower on-state resistance and potentially lower cost and cheaper packaging.
Advantage 2: The GaN device has easy access to all terminals because of lateral configuration. It is easier to co-package with a drive, protection or controller circuit.

Disadvantage 1: Initial cost of the wafers. The technology is still expensive as it requires GaN layers to be grown on silicon substrates.
Disadvantage 2: Because of the lateral configuration, the current capability is limited when compared to a vertical device. [20%]

Question 1, on the SMPS design and calculation of losses was attempted by 12 undergraduates and 4 graduates with an average of 77.08% for undergraduates. This question was virtually answered by all the candidates to a very high standard. It was pleasing to see that the candidates had good knowledge of SMPS systems and calculation of losses in an IGBT.. Most candidates were able to do the theoretical part of the question concerning the superjunction. The question was easier than the others.

Question 2 was on the IGBT equivalent circuit and protection circuits. The question was attempted by 6 undergraduates and 1 graduate with an average of 64.17% for undergraduates. The candidates found confusing the use of protection circuits, though there were some brilliant answers. The theoretical part on the equivalent circuit of IGBTs was answered very well.

Question 3 was a 'blue sky' question where the candidates were asked to look at a thyristor using a JFET type gate. This was attempted by 9 undergraduates and 3 graduates. The average mark was 57.22%. This was perceived by the candidates as a difficult question. In spite of that there were some very good answers.

Question 4 was more theoretical and was concerned with the edge terminations and field rings as well as GaN HEMTs and their advantages against silicon MOSFETs.. The question was attempted by 12 undergraduates and all graduates with an average of 69.17% for undergraduates. The question was very well answered by most of the candidates.