4B6 Crib 2018

Q1

(a) The threshold voltage corresponds to the condition (for a p-type semiconductor):

$$n \text{ (at the surface)} = n_s = N_A$$

$$n_s = n_0 \exp\left(\frac{q\psi_s}{kT}\right)$$

where n_0 is the concentration of electronics in the bulk:

$$n_0 = \frac{n_i^2}{N_A}$$

At the threshold:

$$N_A^2 = n_i^2 \exp\left(\frac{q\psi_s}{kT}\right)$$

$$\psi_s = 2\frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$$

The threshold voltage is the voltage V_G to be applied to the gate to achieve the above surface potential ψ_s. [10%]

(b) Since

$$V_G = V_i + \psi_s$$

and

$$\psi_s = 2\frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) = 0.612 \text{ V}$$

$$V_i = -\frac{Q_s}{C_{ox}} = -\frac{Q_B}{C_{ox}} = \frac{d}{\varepsilon_i}(2q\varepsilon_s N_A)^{\frac{1}{2}} = 1.177 \text{ V}$$

so:

$$V_G = 1.789 \text{ V}$$

[30%]

(c) In this case, the additional charge of the interface states, Q_{it}, much be included:

$$Q_{it} = -\int_{E_V}^{E_C} qD_{it}F(E)dE = -qD_{it}\left(E_{F_s} - E_V\right)$$

where E_{F_s} is the Fermi level at the surface.

$$E_{F_s} - E_V = E_F(\text{bulk}) - E_V + q\psi_s$$

$$E_F(\text{bulk}) - E_V \cong kT \ln\left(\frac{N_V}{N_A}\right)$$

$$Q_{it} = -0.0013 \text{ C m}^{-2}$$

$$V_i = -\frac{Q_{it} - Q_B}{C_{ox}} = 9.16 \text{ V}$$

$$V_G = 9.77 \text{ V}$$ [30%]

(d) The Fermi function is symmetric about the Fermi level, therefore:

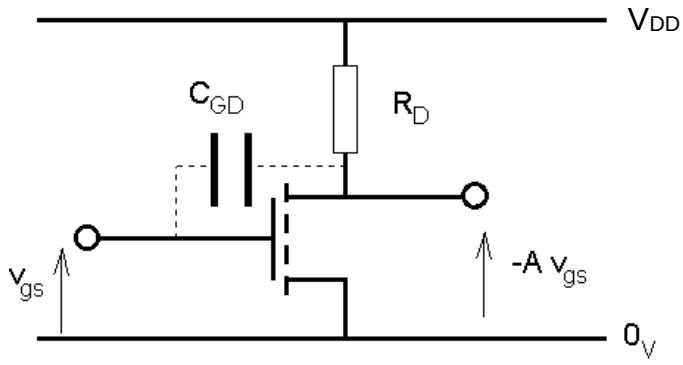
$$\int_{E_V}^{E_C} qD_{it}F(E)dE$$

(i) does not change for D_{it} being constant if the correct $F(E)$ is used; [15%]

(ii) however, for another other D_{it} it will change, in particular if D_{it} increase exponentially towards the conduction band minimum and the difference could be substantial. [15%]

Q2

(a)



The Miller effect related to a MOSFET inverting voltage amplifier is associated to the increase in the effective input capacitance due to the amplification of the coupling capacitance between the input and output terminals, such as the gate and drain of the MOSFET. [30%]

(b) For an inverting amplifier with gain A and Miller capacitance C_{GD}:

(i) the input current due to the Miller capacitance C_{GD} is:

$$i_{in} = v_{gs}\,(1+A)\,j\,\omega\,C_{GD}$$ [10%]

(ii) the effective input capacitance is:

$$C_{eff} = C_{GS} + (1+A)\,C_{GD}$$ [10%]

(iii) the upper 3dB frequency is $f_{upper} \propto 1/C_{input}$, therefore:

$$\frac{f_{upper,with}}{f_{upper,without}} = \frac{C_{GS}}{C_{GS} + (1+A)\,C_{GD}}$$ [20%]

(c) Increase of the effective capacitance at the input can lower the bandwidth of the amplifier, reducing its range of operation to lower frequencies.

The physical origin of Miller capacitance here is the overlap of the gate and drain of the MOSFET. Careful design of the device geometry and control of fabrication process will be able to reduce the Miller capacitance significantly. [30%]

Q3

(a) WRITE : WL set to High (i.e. the transistor to ON state);
Apply a positive(negative) voltage pulse between the BL and the CP, which is sufficiently high to switch the ferroelectric material of the ferroelectric capacitor to a positive(negative) polarisation direction, corresponding to the "1"("0") state;
WL set to Low (i.e. the transistor to OFF state).

READ : WL set to High (i.e. the transistor to ON state);
Apply a voltage pulse of a fixed polarity (either positive or negative) between the BL and the CP;
Use sense amplifier connected to the BL to detect its potential change and determine the value of the ; (The fixed voltage pulse will switch or not switch the polarisation in the ferroelectric capacitor, depending the information state stored in it and resulting a difference in the amount of electric charge dumped from the capacitor to the BL. Because the BL has a finite parasitic capacitance, the difference in the amount of charge translates to the different in the BL potential, which is picked up by the sense amplifier attached to it.)
If the voltage pulse has switched the ferroelectric material, applying a voltage pulse of opposite polarity to switch the polarisation back and restore the originally state of stored information;
WL set to Low (i.e. the transistor to OFF state). [50%]

(b) (i) Remnant polarisation: $Pr = 23\ \mu C\ cm^{-2}$
Coercive field: $Ec = 150\ kV\ cm^{-1}$ [10%]

(ii) The corresponding electric field for +5V is +500 kV cm^{-2} (= +5V / 100nm).

Resulting charge is:
$\Delta Q = \Delta P * Area = (0.25\mu m * 0.25\mu m)\ \Delta P = 6.25 \times 10^{-10}\ cm^2 * \Delta P$

a. For State "1" (positively polarised) with CP=+5V and BL=0V,
$\Delta Q_{"1"} = 6.25 \times 10^{-10}\ cm^2 * \Delta P_{"1"} = 6.25 \times 10^{-10}\ cm^2 * (38+23)\ \mu C\ cm^{-2}$
$= 38 \times 10^{-15}\ C = 38\ fC$ [10%]

b. For State "0" (negatively polarised) with CP=+5V and BL=0V,

$\Delta Q_{"0"} = 6.25\text{x}10^{-10}\ \text{cm}^2 * \Delta P_{"0"} = 6.25\text{x}10^{-10}\ \text{cm}^2 * (38\text{-}23)\ \mu\text{C cm}^{-2}$
$= 9.4\text{x}10^{-15}\ \text{C} = 9.4\ \text{fC}$ [10%]

(iii) Energy consumed due to switching of polarisation from negative to positive direction can be approximated in the order of:

$\Delta E \sim 2*Pr*Ec*\text{Volume} = 2*Pr*Ec*\text{Area}*\text{Thickness}$
$= 2*23\ \mu\text{C cm}^{-2} * 150\ \text{kV cm}^{-1}$
$* 6.25\text{x}10^{-10}\ \text{cm}^2 * 100\text{x}10^{-7}\ \text{cm}$
$= 4\text{x}10^{-14}\ \text{J} = 40\ \text{fJ}$ [20%]

Q4

(a) (i) A magnetic tunnel junction (MTJ) consists of two conductive magnetic layers (Co layers here) with a non-conductive non-magnetic tunnel layer (Al_2O_3 layer here) in between. The magnetisation is usually switchable only in one layer.

CPP configuration: Apply voltage across the two magnetic layers and measure the resulting current which tunnels through the non-conductive layer;

CIP configuration: Apply voltage on the same magnetic layer and measure the resulting tunnelling current. [20%]

(ii) The lower Co layer in the CIP configuration can have effect on the measured current. This is because the non-conductive tunnel layer is thin, in comparison to the electron coherence length. The spin polarisation state of the electrons flow from one electrode to the other can be altered when they are scattered of from the lower Co layer during transportation, resulting a change in scattering coefficient (depending on the magnetisation direction in the lower Co layer) when they return to the upper Co layer, hence the change in the magnitude of the measured current. Note that this is a pure quantum effect without classical correspondence. [20%]

(iii) A bit of information is physically stored in terms of the direction of magnetisations in the upper and lower Co layers. For example, the parallel (anti-parallel) configuration can be referred as State "1" (State "0").

The magneto-resistance in a MTJ (in either the CPP or the CIP configuration) is low (high) when the magnetisation directions in the two magnetic layers are parallel (anti-parallel). Therefore, the stored bit of information can be represented by the two levels of MTJ resistance. [10%]

(b) (i) To write a bit of information is to switch the magnetisation in one of the magnetic layers (the upper one here) to the desired direction.

To avoid switching the half-selected cells, switching is performed by using a combined magnetic field induced by the electric current in the corresponding D-Line and B-Line (neither of them can do the switching on its own as shown on the right in Figure 4).

In the case of writing into B2-W2, using D2 to induce a magnetic field and switching the magnetisation half way and followed by using B2 to induce a separated magnetic field in the desired direction to complete the switching. [30%]

(ii) Select W2 to High (i.e. the transistor to ON state), apply a voltage on B2 and measure the current through it. The current level corresponds to the resistance of the MTJ at B2-W2, hence the bit of information stored in it. [10%]

(iii) A MTJ should be rectangle in shape, so that the magnetisation in the switchable layer only has two easy directions, representing the state of stored binary information. [10%]

Q1 MIS capacitor

Least popular question taken by only 8 candidates. Majority of the candidates did well, showing a good understanding of the principles of MIS capacitors.

Q2 MOSFET and Miller Effect

Second most popular question, taken by 15 candidates. A question answered reasonably well by majority of the candidates. No problem in describing the underlying principles, but some showed a lack of appreciation that the Miller effect was associated with inverting amplifiers.

Q3 FRAM

Most popular question taken by everyone (but one of them, 5492E, did not provide the script sheets for this question, hence the zero mark). Straightforward calculations. Many of the candidates did very well, but some did not mention how the sensing of switch charges is done.

Q4 MRAM

The second least popular question. Taken by only 9 candidates. It appears not easy to cover all the points to get a perfect answer, such as mentioning not only three elements in a GMR device but also their detailed functions.