Engineering Tripos, Part IA, 2018

Paper 3 Electrical and Information Engineering

Solutions

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Part IA Paper 3 Section A crib

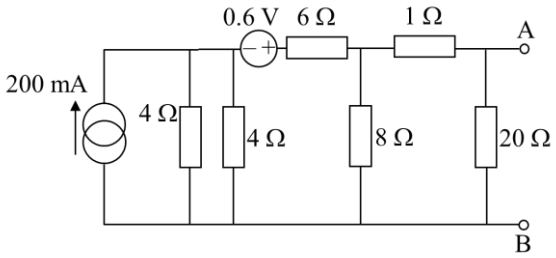
SECTION A

1 **(long)**

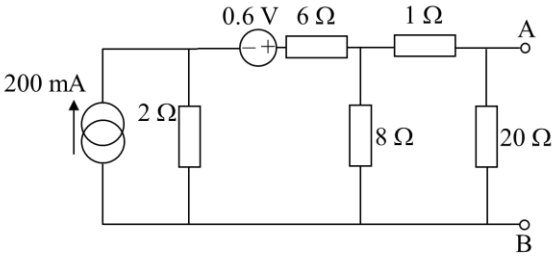
(a) Thevenin's theorem states that as far as the load is concerned, any linear circuit can be represented by an ideal voltage source of voltage V_{th} in series with a resistor of resistance R_{th} in which $V_{th} = V_{oc}$ where V_{oc} is the open circuit voltage. R_{th} is related the V_{oc} and the short circuit current I_{sc} by $R_{th} = V_{oc}/I_{sc}$.

Norton's theorem states that as far as the load is concerned, any linear circuit can be represented as a current source of current I_n in parallel with a resistor R_n in which I_n is equal to the short circuit current I_{sc} and $R_n = R_{th} = V_{oc}/I_{sc}$

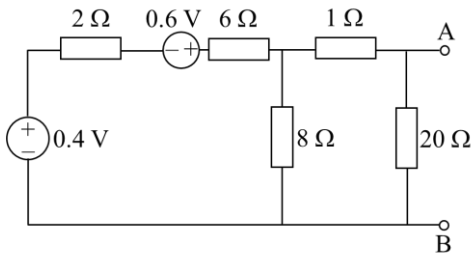
(b) The numbers are chosen so that there is no need for a calculator. Firstly, convert 100 mA current source in parallel with 6 Ω resistor to its Thevenin equivalent, and convert 0.8 V voltage source in series with 4 Ω resistor to its Norton equivalent:



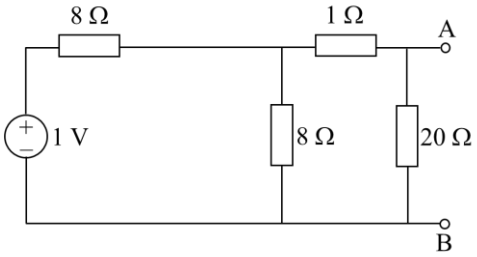
Then, combine the two 4 Ω resistors in parallel:



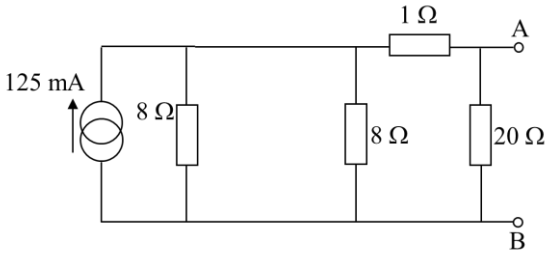
Convert 200 mA current source in parallel with 2 Ω resistor to its Thevenin equivalent:



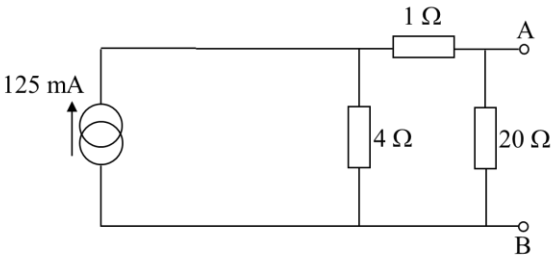
Sum voltage and resistances in series:



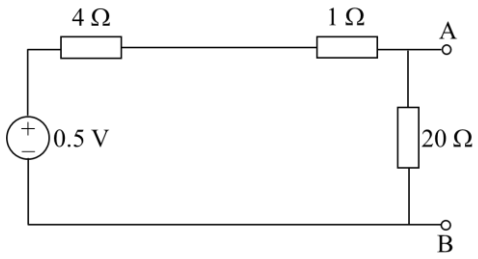
Convert 1 V voltage source and 8 Ω resistor to Norton equivalent:



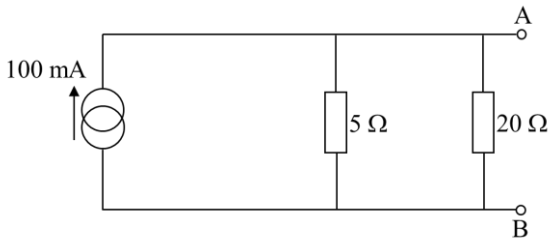
Combine the two 8 Ω resistors in parallel:



Convert 125 mA current source in parallel with 4 Ω resistor to Thevenin equivalent:

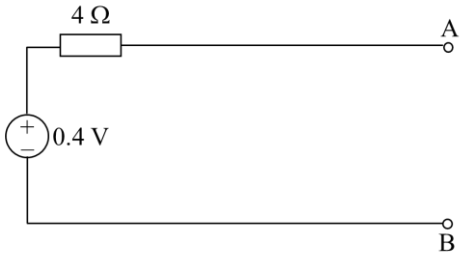


Convert 0.5 V voltage source in series with 5 Ω resistor to Norton equivalent:

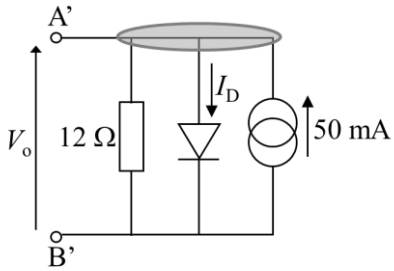


Add 5 Ω and 20 Ω resistors in parallel to achieve **Norton equivalent**:

Convert to **Thevenin equivalent**:



(c)



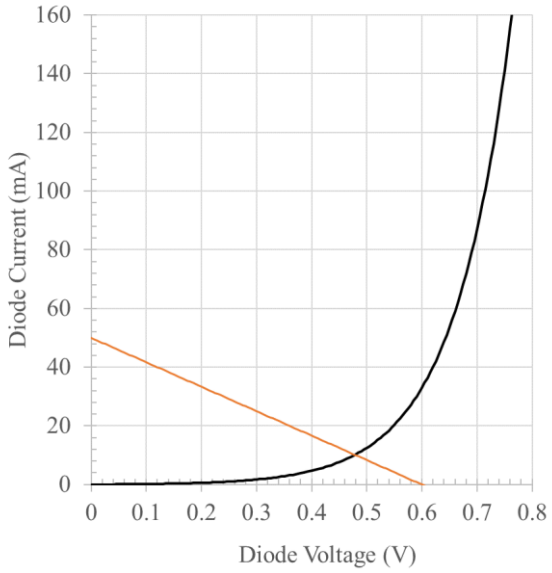
Apply Kirchoff's current law ($\Sigma I = 0$) at the node shaded above:

$$\sum I = 0.05 - I_D - \frac{V_D}{12} = 0$$

Rearrange to obtain the load line:

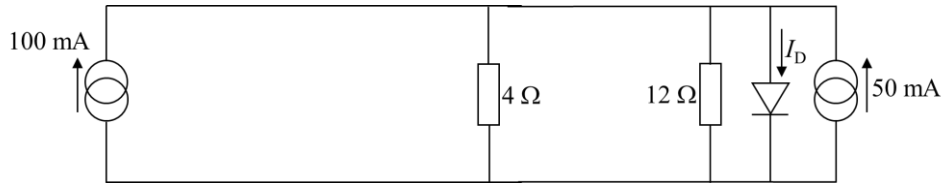
$$I_D = 0.05 - \frac{V_D}{12}$$

Plot the load line and find the intercept:



The intercept between the load line and diode curve occurs at $V_D = V_o = 0.48$ V. This gives V_o.

(d) The circuit becomes:



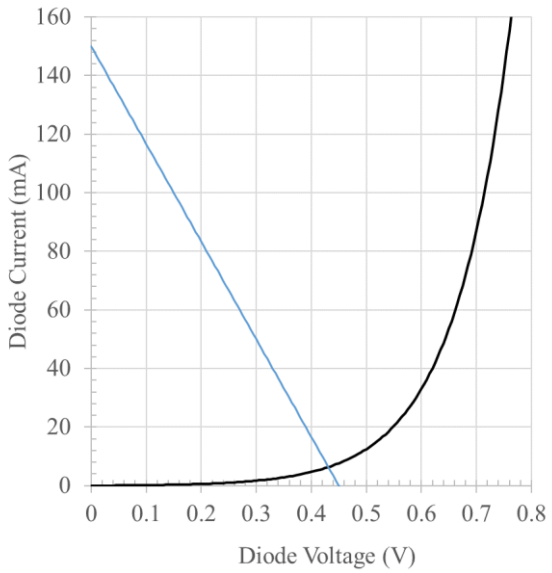
Apply Kirchoff's current law ($\Sigma I = 0$):

$$\sum I = 0.05 + 0.1 - I_D - \frac{V_D}{12\|4} = 0$$

Rearrange to obtain the load line:

$$I_D = 0.15 - \frac{V_D}{3}$$

Plot the load line and find the intercept:



The intercept between the load line and the diode curve occurs at $V_D = V_o = 0.43$ V. This gives V_o.

2 **(long)**

(a) C_{in} and C_{out} are **coupling** capacitors that block dc bias. C_{in} removes any dc component from V_{in} which would otherwise affect the operating point of the amplifier. C_{out} removes the dc component due to the operating point from V_{out}. C_s is a **bypass** capacitor that increases gain by removing ac feedback which would otherwise be generated by the presence of the self-biasing resistor R_2.

(b) At dc all capacitors are open circuits. The voltage across R_2 is given by $I_{ds}\,R_2 = V_s$.

Therefore $R_2 = V_s / I_{ds}$.

Because the gate is at 0 V due to the 10 MΩ resistor, we know that $V_s = -V_{gs} = 2$ V.

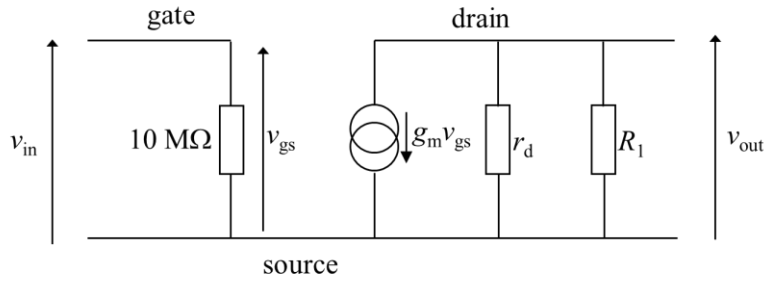
Therefore $R_2 = 2/0.001 =$ **2 kΩ.**

The voltage at the drain $V_d = V_{ds} + V_s = 10 + 2 = 12$ V.

The voltage across R_1 is given by $I_{ds}\,R_1 = V_d$.

Therefore $R_1 = (20-V_d)/ I_{ds} = (20-12)/0.001 =$ **8 kΩ.**

(c) At mid-band all capacitors are short circuits, meaning that R_2 is bypassed.



Input impedance $R_{in} =$ **10 MΩ**

Output impedance $R_{out} = R_1 || r_d = 25k||8k =$ **6.06 kΩ**

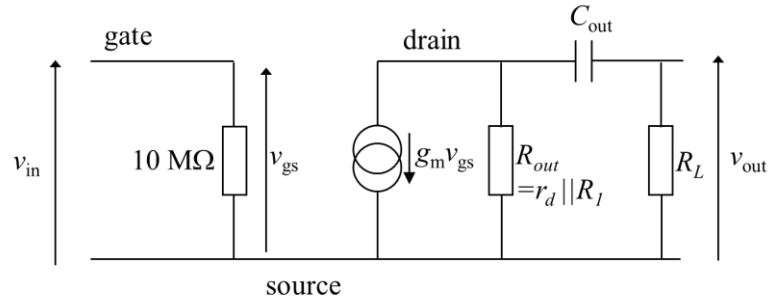
$v_{out} = -g_m v_{gs}(R_1 || r_d)$

Small signal voltage gain = v_{out}/v_{in} = $-g_m v_{gs}(R_1 || r_d)/ v_{gs}$ = -10 × 6.06 = **-60.6**

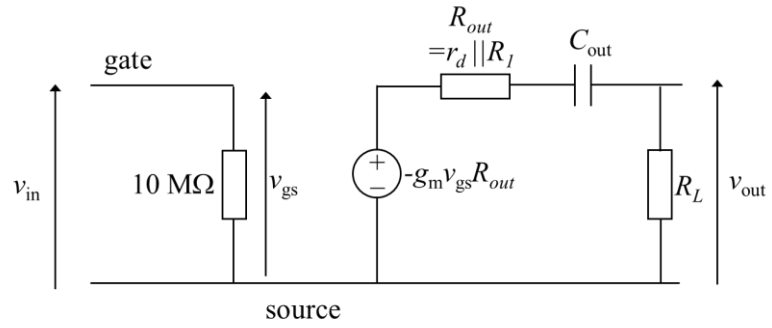
The modulus of v_{out}/v_{in} is **60.6**.

(d)

With C_{out} the circuit becomes:



Taking the Thevenin equivalent of the RHS gives:



$$v_{out} = -g_m v_{gs} R_{out} \frac{R_L}{R_{out} + R_L + 1/j\omega C_{out}}$$

The 3 dB point will be where the real and imaginary parts of the denominator are equal in magnitude, that is, when $R_{out} + R_L = 1/\omega C_{out}$.

The occurs when

$$C_{out} = 1/[\omega(R_{out} + R_L)] = 1/[100 \times 2 \times \pi(6.06 + 10) \times 10^3] = \textbf{99 nF}.$$

(e) Power to the load is maximised when $R_L = R_{out}$ = **6.06 kΩ.**

3 **(short)**

(a) At 513 kHz, the impedance of the inductor is:

$Z_L = j\omega L = j2\times\pi\times513\times10^3\times15.5\times10^{-6} = j50\ \Omega$.

At 513 kHz, the impedance of the capacitor is:

$Z_C = 1/j\omega C = 1/(j2\times\pi\times513\times10^3\times3.1\times10^{-9}) = -j100\Omega$

The total impedance of the circuit is then:

$Z = j50 - j100 + 50 =$ **$50 - j50 = 70.7 \angle -45°$.**

The current is given by:

$$i = \frac{v_{in}}{R_{antenna} + j\omega L + 1/j\omega C} = \frac{0.1}{50 - j50} =$$ **$1.41\ mA \angle 45°$.**

That is the current leads the voltage with phase angle 45°

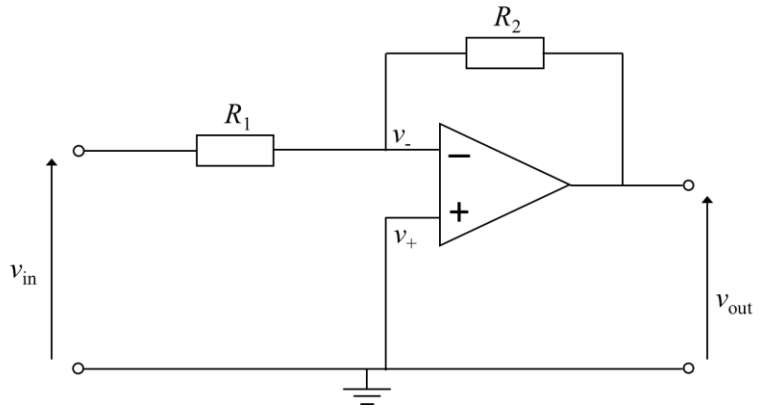
(b)

$$v_{out} = \frac{v_{in}/j\omega C}{R_{antenna} + j\omega L + 1/j\omega C} = \frac{v_{in}}{j\omega C R_{antenna} + 1 - \omega^2 LC}$$

The resonant term is $1-\omega^2 LC$. When this term is zero, the circuit is at resonance. Therefore $C = \frac{1}{\omega^2 L} = \frac{1}{(2\pi\times1.026\times10^6)^2\times15.5\times10^{-6}} =$ **1.55 nF**.

4 **(short)**

(a)



The positive input terminal of the op-amp is connected to ground, so $v_+ = 0$.

The op-amp is ideal, so the two input terminals of the op-amp must be at the same voltage, so $v_- = v_+ = 0$.

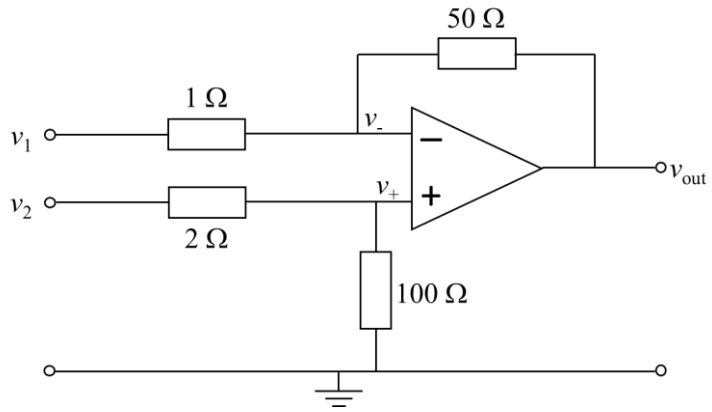
The op-amp is ideal, so no current flows into either input terminal. Therefore, using Kirchoff's current law:

$$\sum I = \frac{v_{in} - v_-}{R_1} + \frac{v_{out} - v_-}{R_2} = 0$$

Substituting $v_- = 0$ into the above and rearranging gives the voltage gain:

$$\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}$$

(b)



The op-amp is ideal, so no current flows into either input terminal. Therefore, using Kirchoff's current law at the positive terminal:

$$\sum I = \frac{v_2 - v_+}{2} + \frac{-v_+}{100} = 0$$

$$\therefore v_2 = \frac{102}{100} v_+$$

(equation 4.1)

The op-amp is ideal, so the two input terminals of the op-amp must be at the same voltage, so $v_- = v_+$. Using Kirchoff's current law at the negative terminal then gives:

$$\sum I = \frac{v_1 - v_+}{1} + \frac{v_{out} - v_+}{50} = 0$$
$$\therefore v_{out} = -50v_1 + 51v_+$$

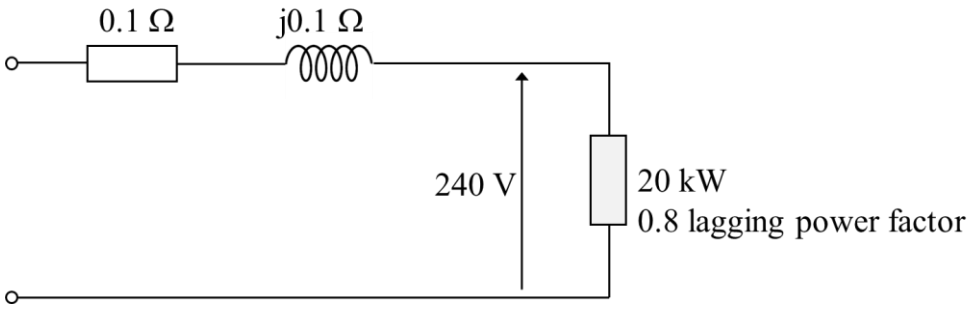
(equation 4.2)

Combining the above gives $v_{out} = -50v_1 + 51\frac{100}{102}v_2 = 50(v_2 - v_1)$

So the circuit amplifies the difference between v_1 and v_2 by a factor of 50.

5 **(short)**

(a)



P = V I cosϕ

Rearranging gives I = P/(V cosϕ) = 20 k /(240 × 0.8) = 104.2 A.

Real power lost in the line = $I^2R = (104.2)^2 \times 0.1 = 1085$ W = **1.085 kW**.

(b)

Power factor correction means correcting power factor to 1.

I = 20 kW/240 V = 83.3 A

Minimum loss = $I^2R = (83.3)^2 \times 0.1 =$ **694 W**.

Apparent power $S = P/\cos\theta = 20k/0.8 = 25$ kVA.

Reactive power $Q = S \sin\theta = 25k \times 0.6 = 15$ kVAR.

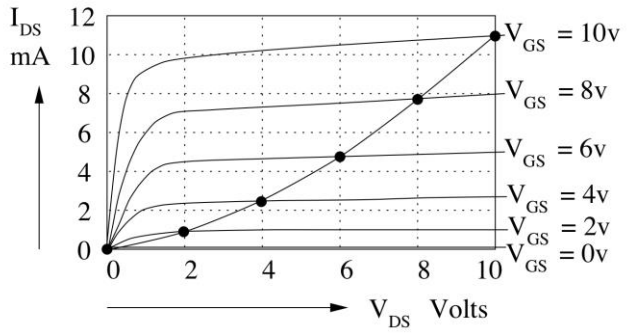
To adjust the power factor, we want the capacitor to give $Q_C = -15$ kVAR.

We know $Q_C = -V^2/X_C = -\omega CV^2$.

Rearranging gives $C = -Q_C/(\omega V^2)$.

Substituting V = 240 V, $Q_C = -15$ kVAR and $\omega = 2\pi \times 50$ Hz gives C = **830 μF**.

6 (**short**)
(a) The NMOS M2 has its gate connected to its drain. Therefore, $V_{GS} = V_{DS}$.
If the relevant points in the given plot are added (figure below), we see a behavior similar to that of a resistor, represented by a straight (but not quite) line (I_{DS} Vs V_{DS}). It has an approximate value of 900ohms - 1 kohms. M2 offers a significantly smaller footprint than a conventional resistor when implemented on a chip. **[5]**



(b) The logic implemented is an Inverter. *This can be explained or shown using a truth table.*
Although it offers a smaller footprint than resistive load based design, the power consumption is still high (compared to CMOS design). For example, when $V_{out} \neq 10$ V, current will flow down the M2 "resistor" and V_{out} = 1v, I_d ~ 9mA, resulting in a power dissipation of ~80 mW. In addition to very high power consumption, the output response of the inverter will also be inferior compared to that of a CMOS implementation. **[5]**

7 (**short**)
(a) Truth table:

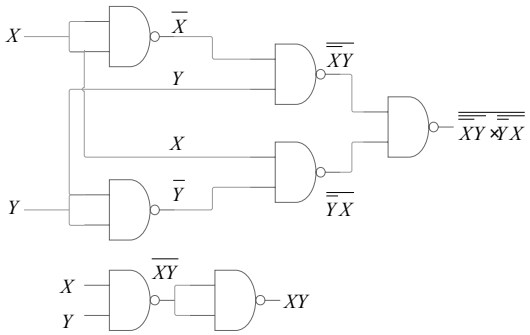
X	Y	Z_1	Z_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

By observation:
$Z_1 = XY$
$Z_0 = X\bar{Y} + Y\bar{X}$ **[4]**

(b) Two gates are sufficient: One two-input AND gate and one two-input XOR gate. **[2]**

(c) NAND gate implementation:

$Z_1 = XY$
$Z_0 = X\bar{Y} + Y\bar{X} = \overline{\overline{X\bar{Y}}.\overline{\bar{X}Y}}$



[4]

8 (**short**)

(a) For the memory chip, 256 kilobyte = number of data lines x $2^{\text{address lines}}$

256 x 1024 x 8 bits = 16 x $2^{\text{address lines}}$

address lines = 17 **[4]**

(b) A microprocessor with 20 address lines can take eight of these memory chips. The most significant 3 lines will be used to address these individual chips. The least significant 17 lines will used for addressing within those individual chips.

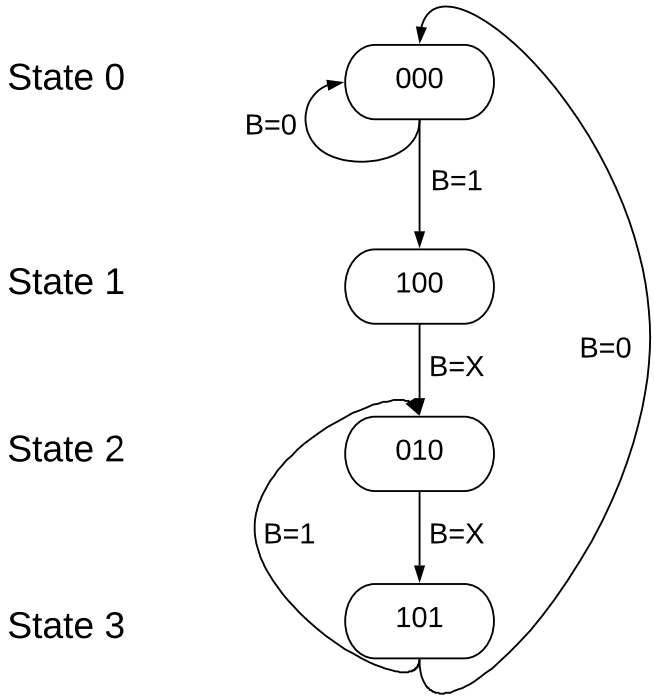
The address ranges of these chips in hexadecimal format:

Chip #	A19	A18	A17	A16	A0-A15	Hex
1	0	0	0	*0*	0	00000
	0	0	0	*1*	1	1FFFF
2	0	0	1	*0*	0	20000
	0	0	1	*1*	1	3FFFF
3	0	1	0	*0*	0	40000
	0	1	0	*1*	1	5FFFF
4	0	1	1	*0*	0	60000
	0	1	1	*1*	1	7FFFF
5	1	0	0	*0*	0	80000
	1	0	0	*1*	1	9FFFF
6	1	0	1	*0*	0	A0000
	1	0	1	*1*	1	BFFFF
7	1	1	0	*0*	0	C0000
	1	1	0	*1*	1	DFFFF
8	1	1	1	*0*	0	E0000
	1	1	1	*1*	1	FFFFF

[6]

9 (**long**)

(a) The system has three variables: H, V and M. Considering the states of the system represented as "HVM", we can draw the following state diagram.



[5]

(b) There are four states. Therefore, the number of bistables required will be 2. However, there are three variables (H,V,M). We can minimize these to a two-variable (a,b) system using the following table:

a	b	H	V	M
0	0	0	0	0
0	1	1	0	0
1	0	0	1	0
1	1	1	0	1

By observation:
$H = b$
$V = a\bar{b}$
$M = ab$

The state transition table:

			B=0			B=1		
H	V	M	H	V	M	H	V	M
0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	1	0
0	1	0	1	0	1	1	0	1
1	0	1	0	0	0	0	1	0

This can be converted to the following:

		B=0		B=1	
a	b	a	b	a	b
0	0	0	0	0	1
0	1	1	0	1	0
1	0	1	1	1	1
1	1	0	0	1	0

[12]

(c) Considering JK transitions, the following K maps can be drawn:

J_a	ab			
	00	01	11	10
B 0	0	1	X	X
1	0	1	X	X

Giving $J_a = Q_b$

K_a	ab			
	00	01	11	10
B 0	X	X	1	0
1	X	X	0	0

Giving $K_a = \overline{B}Q_b$

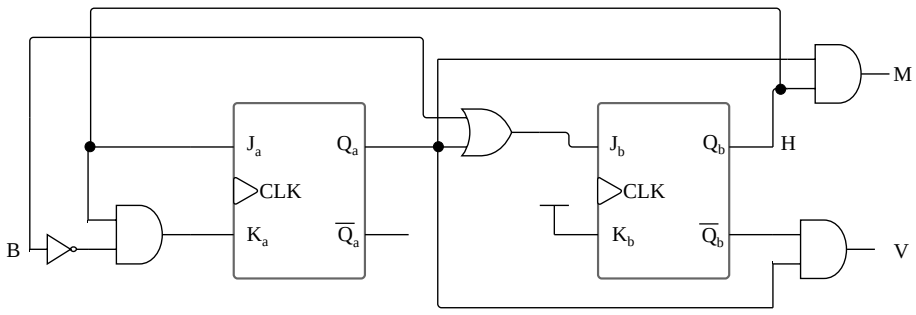
J_b	ab			
	00	01	11	10
B 0	0	X	X	1
1	1	X	X	1

Giving $J_b = Q_a + B$

K_b	ab			
	00	01	11	10
B 0	X	1	1	X
1	X	1	1	X

Giving $K_b = 1$ **[8]**

(d) Circuit implementation:



[5]

Engineering Tripos Part IA 2018
Paper 3: Electrical & Information Engineering
Section C
Cribs

Q10 (short)

First, find the charge stored on one sphere alone. Let this be Q.

from

$$D=\frac{Q}{4\pi r^2}$$

we get:

$$E=\frac{Q}{\varepsilon_0 4\pi r^2}$$

then:

$$V=\int_R^\infty \frac{Q}{\varepsilon_0 4\pi r^2}dr=\frac{Q}{\varepsilon_0 4\pi r}$$ with R the radius of the sphere

Then

$$Q=V\varepsilon_0 4\pi r$$

Now we use the method of images and add as sphere with charge -Q, whose centre is 200mm from the centre of the first sphere. Summing the effects of both spheres we get:

$$E=\frac{Q}{\varepsilon_0 4\pi r_1^2}-\frac{-Q}{\varepsilon_0 4\pi r_2^2}=\frac{2VR}{r^2}=\frac{2\times 60V\times 20mm}{(100mm)^2}=240V/m$$

with $r=r_1=r_2=100mm$

Q11 (short)

(a) Flux density always points in the circumferential direction and at any given radius has constant magnitude. With current flowing out of the paper, the flux density is anticlockwise. Thus, flux density vectors form circles. No flux outside the outer conductor, since net current is zero.

(b) From Ampere's law

$I=2\pi rH$

thus

$$B=\frac{\mu_0 I}{2\pi r}$$

where I is the net current enclosed

Thus, for r=1.5mm, I=1.5A and B= $2\cdot10^{-4}$ T

for r=2.5mm, I=1.5A and B= $1.2\cdot10^{-4}$ T

for r=4mm, I=0, and B=0

Q12(long)

(a)

From the Mawell-Ampere Law:

$$\oint \mathbf{H}\cdot\mathbf{dl}=\int_S \left(\mathbf{J}+\frac{\partial \mathbf{D}}{\partial t}\right)\cdot\mathbf{dS}$$

The rate of change of D is zero and $\int_S \mathbf{J}\cdot\mathbf{dS} = NI$

The cross section of the bar and C shaped bar are uniform, so **H** is constant and parallel to **dl** around the dotted line, hence HL=NI

since

$B=\mu_0\mu_r H$

$$B=\frac{\mu_0\mu_r NI}{L}=\frac{4\pi\times10^{-7}H/m\times1000\times20\times2A}{80mm}=0.628T$$

(b)

The energy per unit volume stored by a magnetic field is $B^2/2\mu$ if B and μ are constant. If the bar moves a small distance δx, then it sweeps a volume $2A\delta x$ in air, where A is the cross sectional area of the C shaped bar. The energy used to move the bar equals the applied force F times the distance δx:

$$F\delta x=\frac{B^2}{2\mu}\ 2A\delta x$$

then

F= $\frac{B^2}{\mu_0}$ A= $\frac{(0.638T)^2}{4\pi \times 10^{-7} H/m}(15mm)^2 = 70.68N$

(c)

The H filed in air (H_a) will differ from that in the iron (H_i). Thus:

$H_aL_a+H_iL_i=NI$

and

$\frac{B_a}{\mu_0} L_a + \frac{B_i}{\mu_0 \mu_r} L_i = NI$

but

$\int_S \mathbf{B} \cdot \mathbf{dS} = 0$, hence B is continuous across a boundary, and $B_a=B_i$

Then

$B = \mu_0 \frac{NI}{L_a + \frac{L_i}{\mu_r}} = 4\pi \times 10^{-7} H/m \frac{20 \times 2A}{4mm + \frac{80mm}{1000}} = 0.0123T$