Version AN/04

EGT3
ENGINEERING TRIPOS PART IIB

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8 May 2017 9:30 to 11

Module 4B21

ANALOGUE INTEGRATED CIRCUITS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book
Attachment: Values of constants and relevant formulae

10 minutes reading time is allowed for this paper

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

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1 (a) Explain what is meant by an ideal voltage source and an ideal current source. [10%]

(b) Sketch the hybrid-π and T-equivalent circuits for a common-base amplifier. [20%]

(c) Shown in Fig. 1 are two common-base amplifiers, driven by (a) an ideal voltage source and (b) an ideal current source, respectively.

(i) Assuming that each circuit has been properly biased, and that the biasing networks, although not indicated in Fig. 1, do not affect the small-signal analysis, calculate the output resistance, r_{out} for circuits (a) and (b), using the following data: $r_\pi = 1\ k\Omega$, $r_o = 100\ k\Omega$, and $\beta = 100$. [50%]

(ii) Comment on the physical implications of the results for r_{out} for the two configurations. [20%]

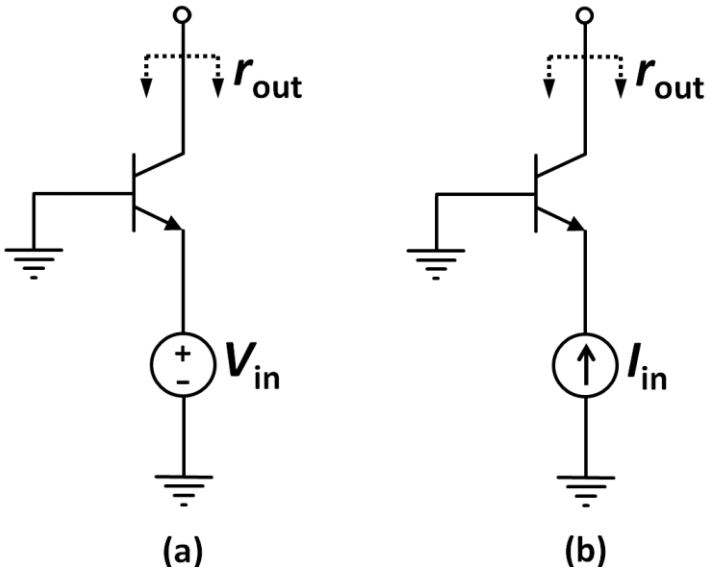

Fig. 1

2 (a) With the aid of a device schematic, describe the main sources of capacitances, and their typical values, that influence high frequency performance for a transistor fabricated in one-micron technology. [25%]

(b) Show that the transistor's unity gain frequency (ω_T) can be approximated as $\omega_T = g_m/(C_{gs} + C_{gd})$, where g_m is the transconductance, and C_{gs}, C_{gd} the gate-source and gate-drain capacitances, respectively. Sketch the simplified equivalent circuit used in your calculation. [20%]

(c) Consider an integrated circuit common-source amplifier with the following parameters: $g_m = 1.25$ mA/V, $C_{gs} = 20$ pF, $C_{gd} = 5$ pF, $C_L = 25$ pF, and effective source and load resistances, $R_s = 10$ kΩ and $R_L = 10$ kΩ.

(i) Estimate the 3 dB frequency f_H of the circuit. [20%]

(ii) What is the gain-bandwidth product? [15%]

(iii) Describe two ways of trading the dc gain for bandwidth. [20%]

3 (a) What is a multi-stage amplifier? [10%]

(b) State five functions that the different stages provide in a multi-stage amplifier. [20%]

(c) In the multi-stage amplifier shown in Fig. 2, fabricated using *0.8-µm* technology, calculate:

(i) $I_D, |V_{OV}|, V_{GS}, g_m$ and r_o for each transistor in circuit.
Tabulate your values. [40%]

(ii) The dc open-loop voltage gain. [10%]

(iii) The input common-mode range. [10%]

(iv) The output voltage range. [10%]

The circuit has the following parameter values:

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
Aspect ratio, *W/L*	20/0.8	20/0.8	5/0.8	5/0.8	40/0.8	10/0.8	40/0.8	40/0.8

I_{REF} = 90 µA, V_{tn} = 0.7V, V_{tp} = -0.8V, $\mu_n C_{ox}$ = 160 µA/V^2, $\mu_p C_{ox}$ = 160 µA/V^2, V_A = 10V, $V_{DD} = V_{SS}$ = 2.5V

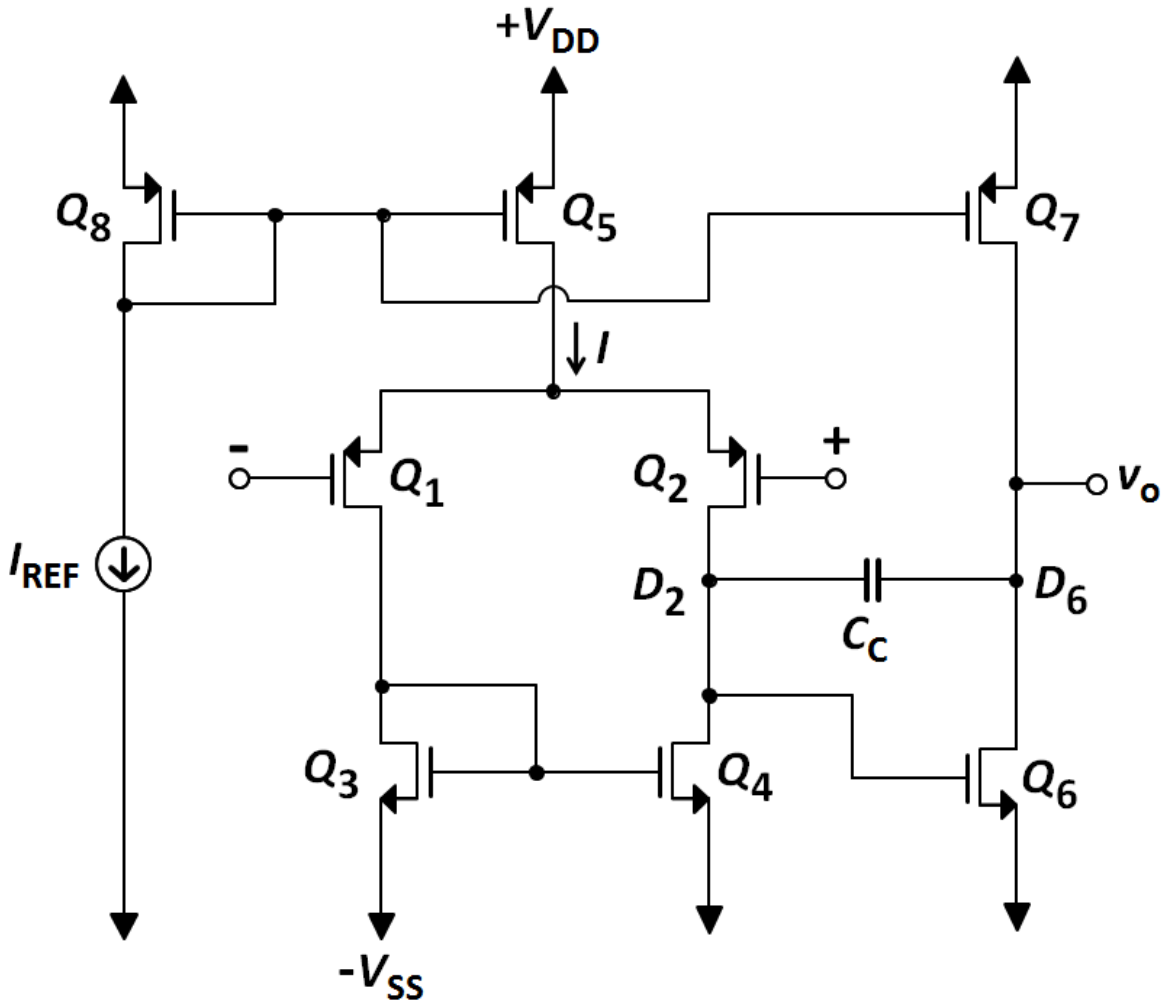

Fig. 2

4 (a) Give a short account of the approaches available for implementation of integrated Digital to Analogue Converters (DACs). Your account should refer to designs based on current and charge scaling, and should draw attention to performance limitations that arise from the use of integrated architectures. Use diagrams where these clarify your explanations, but note that complete DAC schematics are not expected. [40%]

(b) Figure 3 shows a simplified circuit for a four-bit charge-scaling DAC in which the array of capacitors, whose values are all multiples of a standard capacitance C, is split into two separate sections coupled by an attenuation capacitor C_A. The switches are implemented as transistors, each being controlled by a corresponding input signal. Signals D_0 to D_3 represent a binary input data word; D_3 is the most significant bit. When any data input bit is set to 1, the corresponding switch couples the capacitor controlled by it to the voltage reference V_{REF}.

(i) What is the purpose of the switches labelled *Reset* in Fig. 3? Describe the nature of the signals needed to control their state. [10%]

(ii) For the 4-bit converter shown in Fig. 3, the output voltage observed when D_3 is set to logic 1, and D_0, D_1 and D_2 are set to logic 0, is exactly $V_{REF} / 2$. By applying charge balance considerations, determine the correct value for the attenuation capacitor C_A in terms of C for this to be so. [20%]

(iii) With the value of C_A determined in (ii) above, find (in terms of V_{REF}) the output voltage observed when D_1 is set to logic 1 and all other data inputs are logic 0. [10%]

(iv) State, with reasons, any advantages that might arise from the use of a split-array architecture of this kind. [10%]

(cont.

(v) What factors limit the precision that can be achieved in a design of this kind, and how can these be addressed in a practical implementation? [10%]

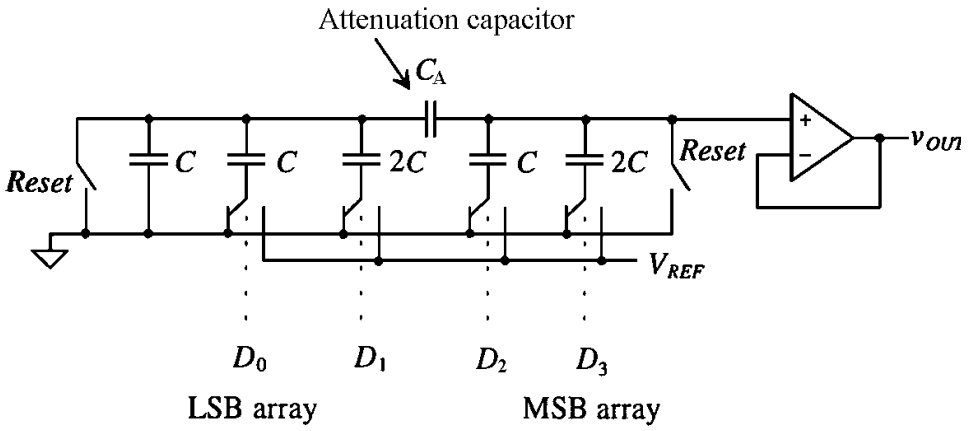

Fig. 3

5 (a) Name three sources of noise that are commonly found in integrated circuit components. [20%]

(b) Sketch the small signal equivalent circuit of a field effect transistor indicating the various noise sources, along with their descriptions, and its output noise voltage power spectral density. [20%]

(c) Assuming that the MOSFET is connected to a low impedance signal source and a load R_L = 1 kΩ, what is its equivalent input noise at high enough frequencies where *1/f* noise is negligible? Assume g_m = 1.25 mA/V and a voltage gain, A_V = 200 that is reasonably flat over a broad range of frequencies. [30%]

(d) What is meant by the noise figure of an amplifier? [10%]

(e) Three amplifiers A, B and C to be connected in cascade have the following noise figures (NF): NF_A = 1.7, NF_B = 2.0 and NF_C = 4.0. Taking into consideration the order in which the amplifiers must be connected, what is the lowest overall noise figure attainable? [20%]

END OF PAPER

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FORMULA SHEET

Bipolar Junction Transistors:

$i_C = \alpha i_E \quad i_C = \beta i_B \qquad i_B = (1-\alpha) i_E \qquad i_E = (\beta+1) i_B$

$\beta = \frac{\alpha}{1-\alpha} \quad \alpha = \frac{\beta}{\beta+1}$ q = 1.6 x 10^{-19} couls, $V_T = \frac{kT}{q} = 25\ mV\ at\ 300K$

$g_m = \frac{I_C}{V_T} \quad r_\pi = \frac{V_T}{I_B} \qquad r_e = \frac{V_T}{I_E}$

$r_o = \frac{V_A}{I_C}$

MOSFETs:

$i_D = K[2(v_{GS} - V_t)v_{DS} - v_{DS}^{\ 2}]; \qquad i_D = K(v_{GS} - V_t)^2 = \frac{k'}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2$

$K = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right) \quad k' = \mu C_{ox} \qquad g_m = 2K(v_{GS} - V_t) \qquad r_o = \frac{|V_A|}{I_D}$

Differential Amplifiers:

$v_o = A_d v_d + A_{cm} v_{cm} \qquad CMRR = 20\log|A_d / A_{cm}|$

$A_{cm} = \frac{v_o}{v_{cm}}$ ***or*** $A_{cm} = \frac{\Delta R_D}{2R}$; $\qquad A_d = \frac{v_o}{v_d} = g_m R_D$ ***or*** $A_d = \frac{\Sigma R_C}{\Sigma R_E}$

BJT small signal operation: $i_{C1} \approx \frac{\alpha I}{2} + \frac{\alpha I}{2V_T}\frac{v_d}{2} \qquad i_{C2} \approx \frac{\alpha I}{2} - \frac{\alpha I}{2V_T}\frac{v_d}{2}$

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$$R_{id} = 2(\beta+1)(r_e + R_E) \qquad R_E = \textit{emitter resistance}$$

FET small signal operation: $$i_{D1} \approx \frac{I}{2} + \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2} \qquad i_{D2} \approx \frac{I}{2} - \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2}$$

Millers Theorem: $$C_{eq} = C_{bridge}(1-K) \qquad K \equiv \frac{V_2}{V_1}$$

2016-2017 4B21 NUMERICAL ANSWERS

Question 1 (c) (i) (a) 100 kΩ (b) 10.1 MΩ

Question 2 (c) (i) 181.9 kHz (ii) 2.3 MHz

Question 3 (c) (i) Values of I_D, $|V_{OV}|$, V_{GS}, g_m and r_o

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
I_D (μA)	45	45	45	45	90	90	90	90
V_{OV} (V)	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
V_{GS} (V)	1.1	1.1	1	1	1.1	1.1	1.1	1.1
g_m (mA/V)	0.3	0.3	0.3	0.3	0.6	0.6	0.6	0.6
r_o (kΩ)	222	222	222	222	111	111	111	111

(ii) 1109 V/V (iii) 1.1V (iv) –2.2V to +2.2V

Question 4 (b) (ii) 4C/3 (iii) $V_{REF}/8$

Question 5 (c) 8 nV/√Hz (e) 2.475