Version FU/3

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Monday 24 April 2017   9.30 to 11

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Module 4B2

POWER MICROELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1   (a)   Explain what is meant by the active and the deep saturation regions in a high voltage Bipolar Junction Transistor (BJT). Sketch the BJT structure and show the excess charge and the depletion layer in these regions.   [25%]

(b)   Fig. 1 shows the waveforms of a BJT switch in a simplified resistive switching circuit. The switch operates at a switching frequency $f = 10$ kHz with a duty cycle $D = 50\%$. The other parameters are: line voltage $V_{dc} = 250$ V, off-state leakage current $I_{OFF} = 3$ mA, on-state collector current $I_C = 10$ A, on-state base current $I_B = 8$ A, collector-emitter on-state voltage drop $V_{CE} = 2$ V, base-emitter on-state voltage drop $V_{BE} = 0.7$ V, turn-on delay time $t_d = 0.5$ μs, turn-on current rise time $t_r = 1$ μs, turn-off delay time $t_s = 5$ μs, turn-off current fall time $t_f = 3$ μs.

    (i)   Estimate the static, switching and total power losses in the switch.   [40%]

    (ii)   Plot the instantaneous power vs time for one period.   [25%]

    (iii)   Calculate the power loss due to the base current.   [10%]
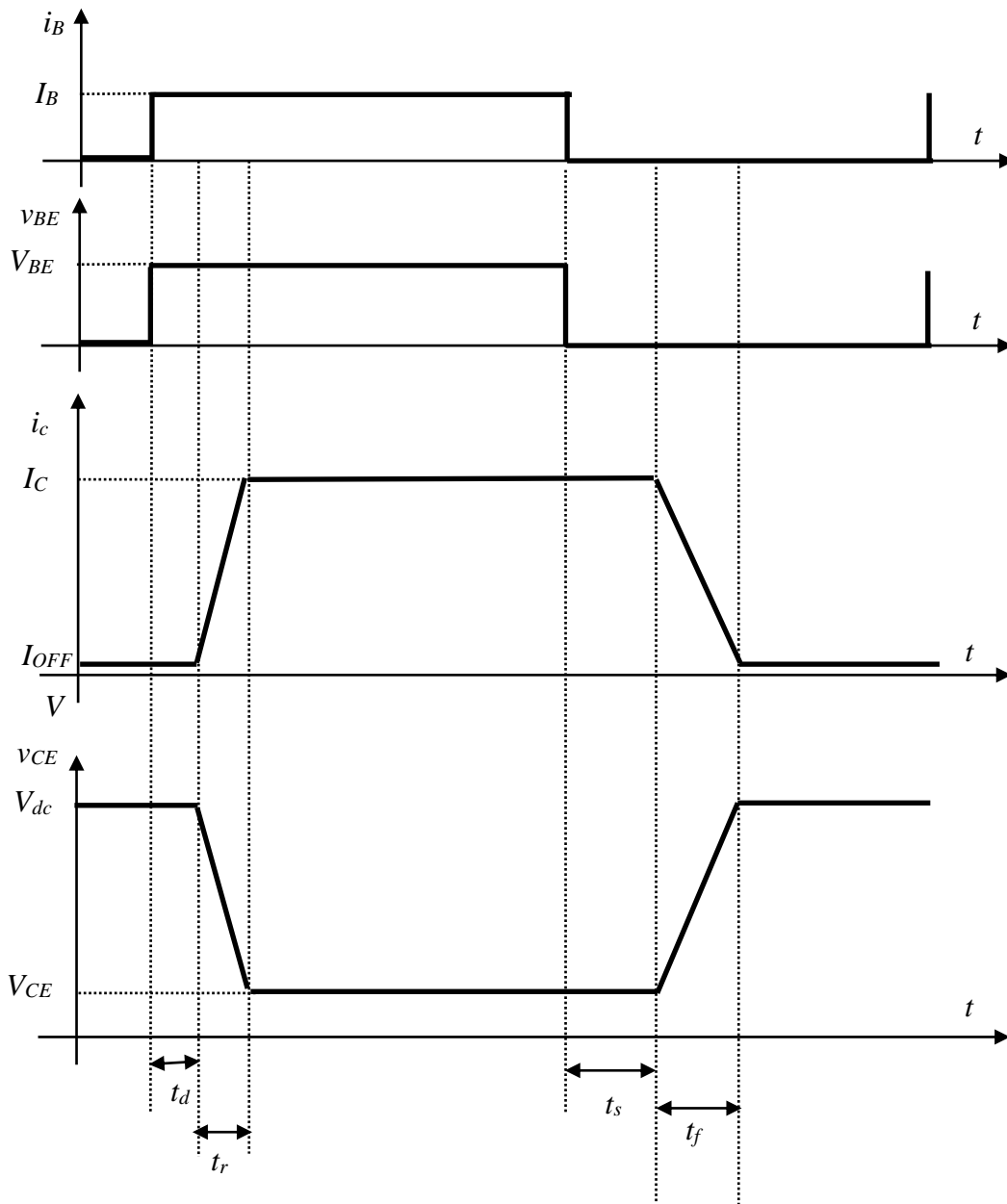
(cont.

Fig. 1 (not to scale)

2   (a)   Explain the latch-up effect in Insulated Gate Bipolar Transistors (IGBTs). Draw an IGBT equivalent circuit that includes the parasitic latch-up elements. Give two solutions to improve the latch-up immunity in IGBTs.   [30%]

(b)   Fig. 2 shows the equivalent circuits of two lateral MOS-bipolar devices.

   (i)   Explain briefly their operation and draw their static I-V characteristics, highlighting the differences between the two structures.   [35%]

   (ii)   Draw the cross-section of the two structures corresponding to the equivalent circuits shown in Fig. 2 (a) and (b). Note that the second circuit in Fig. 2 (b) describes a novel structure.   [35%]
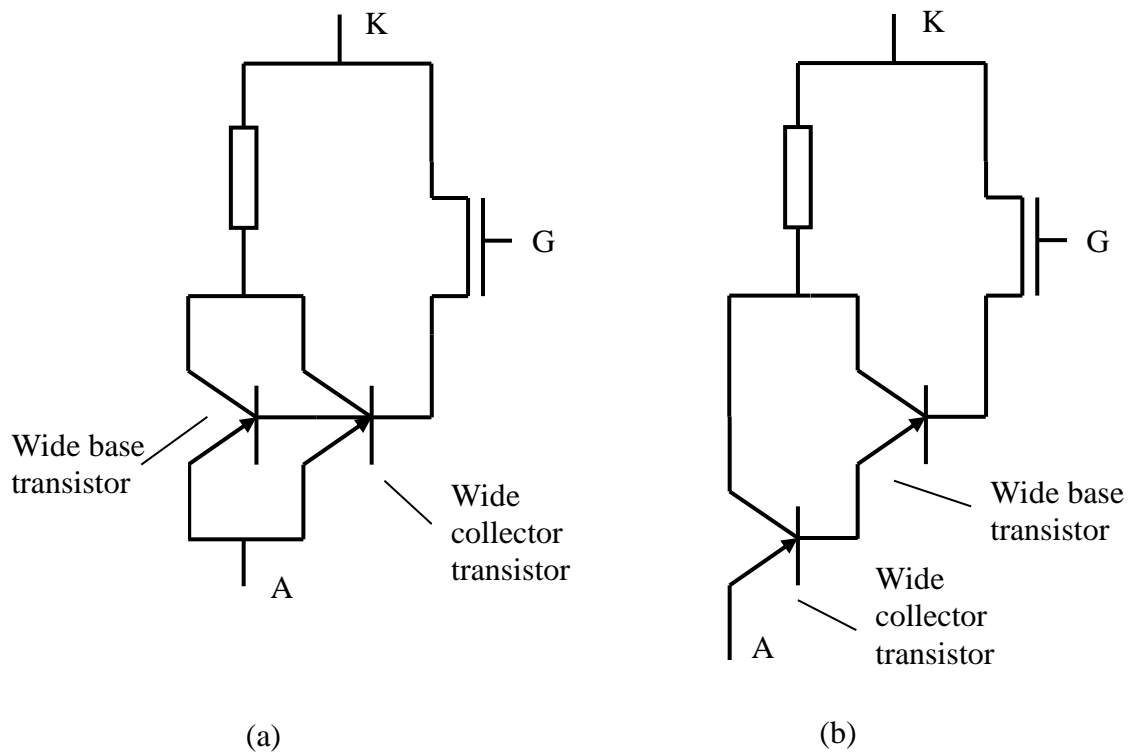

(a)   (b)

Fig. 2

3   The cell structure in Fig. 3 is a junction controlled power device.

(a)   Explain its operation during on-state, off-state, turn-on and turn-off.   [35%]

(b)   Draw an equivalent circuit for the device and the output characteristics.   [30%]

(c)   Give one advantage and one disadvantage of this device compared to a conventional Insulated Gate Bipolar Transistor (IGBT).   [10%]

(d)   Draw a termination structure for the device using layers already present in the cell structure. Show schematically the potential contour in the cell and the termination structure.   [25%]
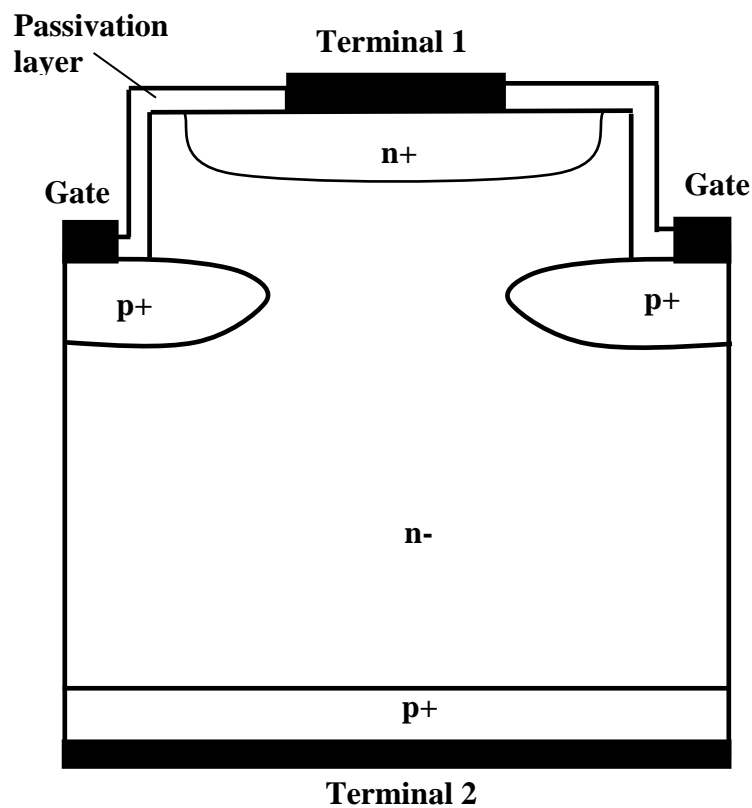

Fig. 3

4   (a)   (i)   Draw the structure of the Cool MOS and explain its advantage in terms of the trade-off between the specific on-state resistance and the breakdown voltage.   [25%]

(ii)   On one set of axes sketch graphs of the drain-source capacitances as a function of the blocking voltage for both the Cool MOS and a conventional Power MOSFET. Explain briefly the different behaviour of the two capacitances at low voltages and high voltages.   [25%]

(b)   (i)   A Power MOSFET and a Cool MOS are to be designed to have the same breakdown voltage V_{br}. Assuming that the critical electric field, E_{cr} remains constant, independent of the doping level, find the optimal doping level and the optimum width of the drift region for the Power MOSFET. What is the optimum width of the drift region for the Cool MOS to deliver the same V_{br}?   [30%]

(ii)   Assume that the doping levels of the Cool MOS n-pillar and p-pillar in part (b) (i) are ten and five times higher than the doping level of the drift region in the Power MOSFET respectively. Find the relative decrease in the specific drift on-state resistance of the Cool MOS with respect to that of the Power MOSFET.   [20%]

You may assume the following equation in the calculation of the breakdown voltage

$$w = \left[\frac{2\varepsilon_r \varepsilon_0 V}{q} \frac{1}{N_D} \right]^{\frac{1}{2}}$$

where w is the depletion region width; N_D is the doping concentration of the drift region, V is the blocking voltage, q is the electronic charge and the other symbols have their usual meaning.

END OF PAPER

Q1: (b) *Total Losses: 27.46%*
Base losses: 2.8W

Q4 (b) (i) $w_{drift} = w = \dfrac{\varepsilon_0 \varepsilon_r E_{CR}}{qN_D}$ for MOSFET

$w_{drift-CoolMOS} = \dfrac{w_{drift-MOSFET}}{2}$

(ii) specific resistance for Cool MOS $= \dfrac{W_{CoolMOS}}{q\mu_n N_{D_{CoolMOS}}} \dfrac{X_n}{X_n + X_p}$

$\dfrac{R_{spCoolMOS}}{R_{spMOSFET}} = \dfrac{1}{10} \times 3 \times \dfrac{1}{2} = \dfrac{3}{20} = 0.15$