Part 1A Paper 3: Electrical and Information Engineering,

EXAMPLES PAPER 4 Linear Circuits & Devices

This examples paper is based on material from lectures 13-18. Where possible, the lectures on which the questions are based are indicated, e.g. [L15]. Questions containing material of tripos standard are marked *.

Small-Signal Models

1. (i) For the FET with the characteristics shown in Fig. 1 below, graphically estimate the values of the small-signal parameters g_m and r_d at the operating point, P.

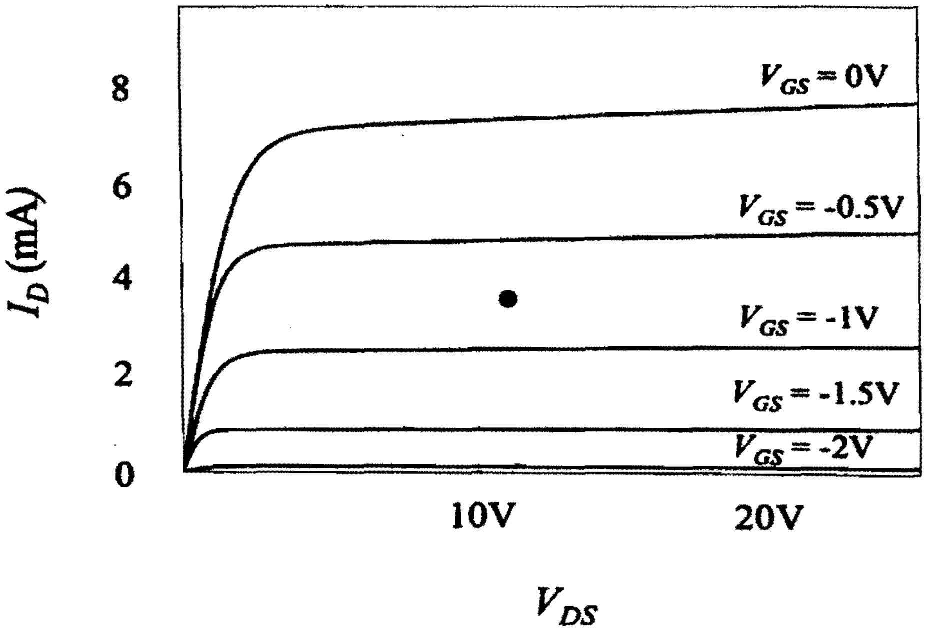


Fig. 1

(ii) The small-signal model of the circuit in Fig. 2(a) is shown in Fig. 2(b). What do R_1, R_2 & R_3 represent? [L13]

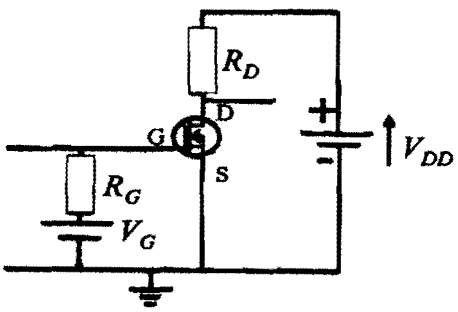
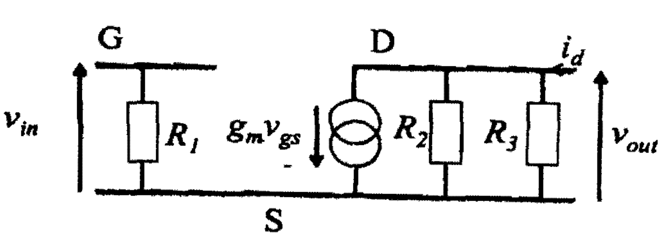


Fig. 2(a)



2(b)

2. An FET has small-signal parameters $gm = 4$ mS and $r_d = 10$ kΩ at the following working point:

$V_{DS} = 8$ V, $I_D = 2.5$ mA, $V_{GS} = 2$ V.

Design a common-mode amplifier circuit using this FET, a + 30V power supply (V_{DD}) and a potential divider to generate the gate bias voltage. Then

(a) Determine the value of the circuit drain resistor and the ratio of potential divider resistances (in the gate bias circuit) that will enable the above operating point to be achieved.

(b) Draw the small-signal equivalent circuit of your design and use it to calculate the small-signal voltage gain of the circuit.

(c) Now assume a further constraint – the input resistance of the circuit must be greater than 100 kΩ. Now determine values of the potential divider resistors that satisfy this requirement. [L13]

3. The circuit shown below in Fig. 3 is known as a source-follower (i.e. the output "follows" the input, so the gain ~1). $R_1 = 2$ MΩ. The FET has small-signal parameters $gm = 5$ mS, $r_d = 50$ kΩ. The operating point for the transistor is $V_{DS} = 7$ V, $I_D = 2.6$ mA, $V_{GS} = -3$ V.

(a) Calculate values for R2 & R3 that will enable the desired operating point to be achieved.

(b) Draw the small-signal equivalent circuit.

(c) Using the small-signal equivalent circuit, calculate the circuit's input resistance, output resistance and voltage gain. [L13]

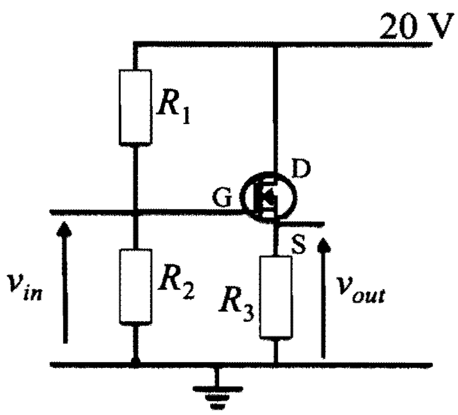


Fig. 3

Coupling capacitors, generic amplifiers

4. A common-source amplifier is shown below in Fig. 4. The small signal-parameters for the FET are

$g_m = 4$ mS, $r_d = 10$ kΩ.

What value of output coupling capacitor, C, is needed between the drain and the load, assuming that the load resistance is 500 Ω, and the voltage across the load can drop to 70% of its maximum value at 20 Hz?

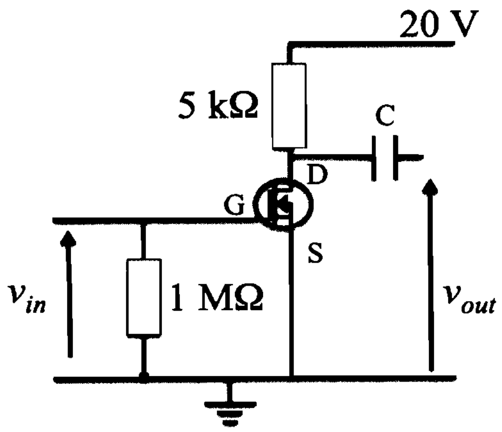


Fig. 4

* 5. In the amplifier circuit of Fig. 5, the field-effect transistor has mutual conductance g_m = 4 mS and an effectively infinite drain resistance, r_d.

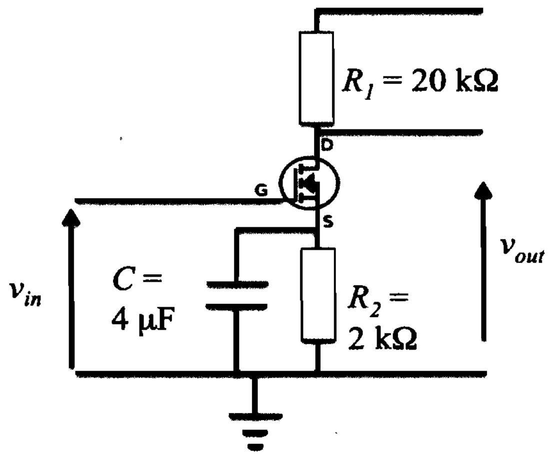


Fig. 5

Derive a general expression for the signal gain v_0/v_1 as a function of g_m, R_1, R_2, C & angular frequency, ω.

Calculate the gain at frequencies of 1.59 Hz, 159 Hz and 15.9 kHz. [L16]

6.

The circuit of an amplifier and its load is shown in Fig. 6

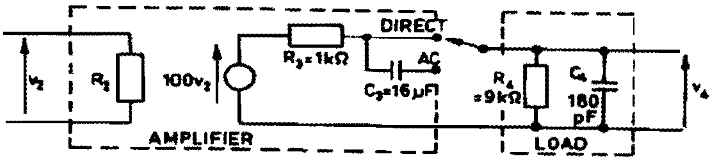


Fig. 6

(a) With the switch between the load and the amplifier in the DIRECT position, as shown, and at a frequency when the effect of C_4 can be ignored, what is the value of the signal voltage gain, v_4/v_2? This is commonly called the mid-band gain.

(b) When the effect of C_4 cannot be ignored, show that the gain v_4/v_2 drops to 70% (or $1/\sqrt{2}$) of its mid-band value at frequency f_4 Hz given by:

$$\frac{1}{2\pi f_4 C_4} = \frac{R_3.R_4}{(R_3 + R_4)}$$

For the circuit values given, find f_4.

(c) Consider the switch between the load and the amplifier to be in the A.C. position and the signal frequency now being very much lower than f_4 so that the effect of C_4 can be ignored. Show that the gain v_4/v_2 drops to 70% (or $1/\sqrt{2}$) of its mid-band value at a frequency f_3 given by:

$$\frac{1}{2\pi f_3 C_3} = R_3 + R_4$$

For the circuit values given, find f_3.

(d) Explain why f_3 and f_4 are also known as the "turnover", half-power or −3dB frequencies.

If R_2 = 1 MΩ and R_4 is the only output load, find the mid-band power gain of the amplifier numerically and in decibels.

If the amplifier is preceded by another stage whose gain is +40 dB and a "volume" control between the two amplifiers is set to −4 dB (i.e. a loss), what is the overall gain in decibels?

[L15]

7. (a) In the circuit of Fig 7(a), if the input voltage, v_{in} is 3 mV rms from a microphone, R_1 = 3 kΩ, R_2 = 500 kΩ, and the Op-Amp is ideal, calculate the output voltage, v_{out}.

(b) In the circuit of Fig 7(b), if the input voltage, v_{in} is 5 mV rms from a microphone, R_3 = 99 kΩ, R_4 = 1 kΩ, and the Op-Amp is ideal, calculate the output voltage, v_{out}.

(c) Now assume that the Op-Amps have finite values of gain, A and input resistance, R_i, but have negligible output resistance. Derive algebraic expressions for the gain v_{out}/v_{in} of each circuit. Show that these expressions reduce to those given in the lectures for ideal op-amps.

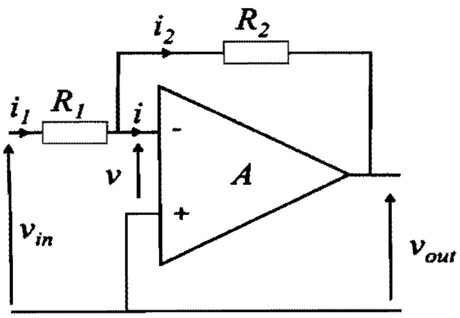
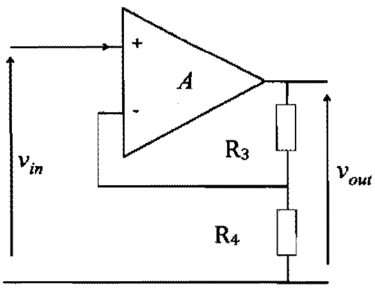


Fig 7(a)



7(b)

8. Figure 8 shows the circuit of a summing amplifier. Assuming that the op-amp is ideal, show that v_{out} is given by:

$$v_{out} = -\left(v_1 \frac{R_f}{R_1} + v_2 \frac{R_f}{R_2}\right)$$

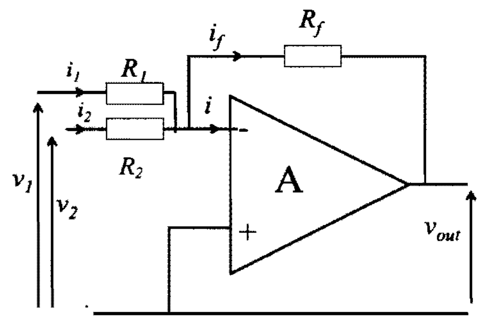


Fig. 8

(a) The summing circuit is required to produce an output $-(200v_1 + 40v_2)$. If $R_f = 100$ kΩ, what values are required for R_1 & R_2, given that the signal sources providing v_1 & v_2 each have an internal output impedance of 200 Ω?

(b) The op-amp is powered from a voltage supply that delivers +V and –V, relative to earth. If v_1 and v_2 have amplitudes 10 mV and 50 mV, respectively, determine the minimum power supply voltages required for the circuit to work correctly.

9. The amplifier circuit shown in Fig. 9 is called a transimpedance amplifier. It is commonly used to amplify very small ac currents and convert them to a voltage. The op-amp used has a gain, A of 10^4, but is otherwise ideal.

(a) Derive an expression for the output voltage per unit input current (this is known as the transimpedance).

(b) Estimate the half-power bandwidth of the circuit for C = 60 pF and R = 10^{10} Ω.

(c) Unfortunately, such a high value of R will have some stray capacitance, C_S, associated with it, which is in parallel with R. If $C_S = 2$ pF, estimate the upper -3dB point for the circuit.

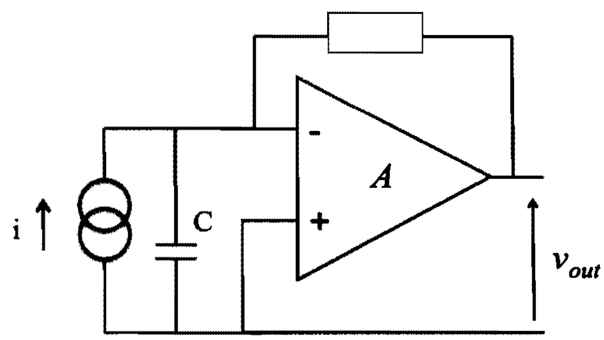


Fig. 9

Answers:

1. (i) 4.6 mS, 40kΩ, (ii) $R_1 = R_G$, R_2 & $R_3 = R_D$ & r_d.
2. (a) 8.8 kΩ, 14, (b) -18.7, (c) 1.5 MΩ from the gate to the power supply line, 107 kΩ from the gate to ground.
3. (a) $R_3 = 5$ kΩ, $R_1=R_2= 2$ MΩ, (c) gain = 0.958, $R_{in} = 1$ MΩ, $R_{out} = 192$Ω.
4. 2.08 μF.
5. $-g_mR_1(1 + j\omega C_2R_2)/(1 + g_mR_2 + j\omega C_2R_2)$, -9, -53.5, -80
6. (a) 90, (b) 1 MHz, (c) 1 Hz, (d) 59.5 dB, 95.5 dB
7. (a) 500 mV rms, (b) 500 mV rms, (c) $-AR_2R_i/(AR_1R_i + R_2R_i + R_1R_i + R_1R_2)$, -> $-R_2/R_1$ when A is large; $A(R_iR_3 + R_iR_4)/(AR_4R_i + R_3R_i + R_4R_i + R_4R_3)$ -> $AR_iR_4/(R_3 + R_4)$ when A is large.
8. (a) $R_1 = 300$ Ω, $R_2 = 2300$ Ω. (b) Power supplies should be at least + 4V and -4V.
9. (a) $-AR/((A + 1) + j\omega CR)$, (b) 2.7 kHz, (c) 8 Hz

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