Engineering Tripos Part IIA, 3B2: Integrated Digital Electronics, 2025-26

Module Leader

Prof OB Akan [1]

Lecturers

Prof OB Akan and Dr M Tang

Lab Leader

Prof OB Akan

Timing and Structure

Lent term. 16 lectures.

Aims

The aims of the course are to:

- Introduce key aspects of integrated digital electronics and its applications as logic devices.
- Introduce design and optimization techniques for combinational and sequential digital logic circuits.
- Introduce programmable logic design and hardware description language (Verilog) concepts.
- Introduce the principles of design and operation of the major digital integrated circuit technologies.
- Discuss the importance of miniaturising digital circuits and their key role in microprocessors, memories and programmable logic devices.

Objectives

As specific objectives, by the end of the course students should be able to:

- Understand the technologies that serve as building blocks to modern digital circuits and know their main applications.
- Analyse and synthesise how LSI circuits are used in logic; Multiplexers, Memory blocks, FPGAs.
- Design sequential logic circuits and finite state machines, and know about the Moore and Mealy models.
- Be familiar with Verilog hardware description language and be able to write code for basic circuits.
- Be familiar with the architecture and programming of modern FPGA devices and the design flow involved.
- Design synchronous circuits and use FPGAs for design of sequential networks.
- Appreciate the drive to miniaturise digital circuits and understand how this has improved performance and reduced cost.
- Know the definitions for noise margins, rise times, fall times and transfer characteristics for digital circuits.
- Be aware of the two operating regions (saturation and non-saturation) of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) and understand how the equations for the two regions are used to design and estimate the performance of digital circuit
- Be familiar with CMOS IC fabrication, layout and simulation fundamentals
- Appreciate the evolution of MOSFET inverters from the resistive load inverter through the enhancement and depletion transistor load inverters to the CMOS inverter.
- Plot the transfer characteristics and calculate the rise times for NMOS and CMOS inverters.

- Know the basic gate circuits for NMOS and CMOS logic and be able to compare their performance.
- Understand CMOS combinational logic gates such as NAND, NOR, XOR, and their delay and power analysis
- Understand CMOS designs of bistable circuit, SR latch, JK flip-flops, D flip-flops and latches and clocking strategies
- Understand the operating principles and design challenges of semiconductor memory circuits
- Be familiar with emerging topics in integrated digital electronics such as FinFETs, GAAFETs, 3D ICs, chiplets

Content

Part I: Logic Circuits & System-Level Digital Design (Lectures 1–8)

Lecture 1 — Introduction to Logic Circuits and Digital Systems

- Boolean algebra revision
- Logic gate synthesis using NAND/NOR
- Overview of logic minimization and combinational networks

Lecture 2 — Verilog Basics and Design Tools

- Verilog syntax, simulation vs. synthesis
- Design units: entities and architectures
- Introduction to FPGA synthesis flow

Lecture 3 — Combinational Circuit Design

- Multiplexers, decoders, priority encoders
- Boolean function implementation
- Lookup tables and hardware mapping in FPGA logic blocks

Lecture 4 — Sequential Logic Fundamentals

- Flip-flops: D, T, JK, SR
- Counters and registers
- Clocking, timing diagrams, basic FSMs

Lecture 5 — FSM Design in Verilog

- State diagram ? Verilog implementation
- Hierarchical design and testbenches
- Case study: traffic light controller or vending machine

Lecture 6 — Programmable Logic Devices

- PLDs, CPLDs, FPGAs
- FPGA architecture overview
- Internal LUT, flip-flop, and routing structure

Lecture 7 — Datapath Elements and Control Logic

- Adders, multiplexers, ALUs, accumulators

- Memory blocks and register files
- Control unit design

Lecture 8 — Digital Signal Processing Case Study

- FFT pipeline overview
- Signal flow and parallelism
- Lab/demo using FPGA FFT IP core in Verilog FPGA design

Part II: Digital Integrated Circuits & CMOS Design (Lectures 9–16)

Lecture 9 — Introduction to CMOS-based Digital Design

- CMOS vs. other logic families
- Structure of digital ICs: cell libraries, standard cells
- Definitions of noise margins, definitions of transient characteristics (rise/fall times, delay), power estimation.

Lecture 10 — MOS Transistors

- MOSFET structures and operation modes
- Threshold voltage, current-voltage characteristics, velocity saturation

Lecture 11 — Fabrication, Layout and Simulation

- IC photolithography, patterning of transistors and wires, layout basics.
- SPICE simulation of MOS devices
- Interconnect and IC design metrics: RC modelling, delay estimation, scaling effects, Power, Performance, and Area (PPA) metrics, signal integrity: crosstalk, ground bounce

Lecture 12 — CMOS Inverter Design and Analysis

- Voltage transfer characteristics (VTC), noise margins and layout
- Power consumption: dynamic vs. static
- Delay analysis of CMOS inverters

Lecture 13 — CMOS Combinational Logic Gates

- NAND, NOR, XOR using CMOS
- Transistor sizing and fan-in/fan-out effects
- Delay and power analysis of CMOS gates

Lecture 14 — CMOS Sequential Circuits

- CMOS designs of bistable circuit, SR latch, JK flip-flops, D flip-flops and latches
- Clocking strategies: edge-triggering, pipelining

Lecture 15 — Semiconductor Memory Circuits

- Memory organisation
- Static ROM and RAM cell designs and operation
- Peripheral circuits (CMOS tri-state buffers, Schmitt triggers)

Lecture 16 — Emerging Topics in Digital Electronics

- FinFET structure and motivation: short-channel e?ects, gate control, scaling
- Comparison of planar CMOS vs. FinFET and impact on digital ICs
- Gate-all-around FETs (GAAFETs), 3D ICs, chiplets

Coursework

[illegible] of programmable logic technology. The boards are DE1-SoC by Terasic using Altera SoC FPGAs and donated by Terasic under Intel FPGA University Programme.

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Students will have the option to submit a Full Technical Report.

Booklists

Please refer to the Booklist for Part IIA Courses for references to this module, this can be found on the associated Moodle course.

Examination Guidelines

Please refer to Form & conduct of the examinations [2].

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