Engineering Tripos Part IIA Project, GB3: RISC-V Processor, 2025-26

Leader

Dr Matthew Tang [1]

Timing and Structure

Fridays 9-11am plus afternoons, and Tuesdays 11-1pm

Prerequisites

3B2 (essential). Experience with Linux command line tools and Github (desirable)

Aims

The aims of the course are to:

- practise digital system modelling techniques using Verilog HDL
- obtain hands-on experience working with FPGAs and their synthesis tools
- explore fundamental concepts in computer architecture through the study and implementation of RISC-V instruction set architecture (ISA)
- perform evaluation and verification of a microprocessor core on FPGAs, in a team environment

Objectives

As specific objectives, by the end of the course students should be able to:

- model digital systems effectively using the Verilog hardware description language
- use design tools for FPGAs for synthesis, simulation and programming
- comprehend a simple microprocessor design and realise improvement in performance, power or area
- systemically evaluate and verify a microprocessor

Content

In this project, the students will be working on improving a simple RISC-V processor in terms of performance, power or area when it is implementation on an iCE40 FPGA. For the first two weeks, the students will be investigating the available hardware resources on the FPGA and learning to model and map a digital system using the Verilog HDL. Then they will be guided to explore the basics of computer architecture through studying the given processor. They will also practise evaluating of the processor implementation for the performance, power and area. In the second half, the groups of three students have the liberty to identify and realise possible improvements for the processor core. For example, pipelining, caching, out-of-order execution, co-processing units are popular options for high performance processors. They will propose, implement, verify and evaluate their improvement and detail the process in the report.

This project will provide you with the opportunity to gain hands-on experience with FPGA, HDL modelling, computer architecture.

Week 1

Introduction to the project. FPGA device and design tools. Measurements with FPGA.

Week 2

Basic computer architecture. RISC-V software tool chain. FPGA implementation of RISC-V processor. Baseline measurements/records.

Week 3

Discussion and proposal of ideas. Preliminary study and implementation. Debugging.

Week 4

Finalised core improvement. Verification, evaluation and optimisation.

Coursework

Coursework	Due date	Marks
Baseline measurements Proper implementation of the given design and records of measurements	TBA	15
Interim presentation Explain the idea of improving the provided RISC-V processor core in terms of performance, power or area	TBA	25
Final report Summarise the achievement of the project. Outline the personal role in group. Reflect on the lesson learned.	4pm Thursday 11 June	40

Booklists

1. Computer Organization and Design RISC-V Edition: The Hardware Software Interface, David A. Patterson, John L. Hennessy, 978-0128122754
2. RISC-V Instruction set manual: https://github.com/riscv/riscv-isa-manual [2]

Examination Guidelines

Please refer to Form & conduct of the examinations [3].

Last modified: 01/12/2025 07:14

Links
[1] mailto:wct26
[2] https://github.com/riscv/riscv-isa-manual
[3] https://teaching.eng.cam.ac.uk/content/form-conduct-examinations