Engineering Tripos Part IIB, 4B28: Very large-scale integration (VLSI), 2024-25

Leader

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Lecturer

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Timing and Structure

Michaelmas term. 75% exam / 25% coursework

Prerequisites

3B2 assumed, 3B5 useful.

Aims

The aims of the course are to:

- provide fundamental knowledge and analytical skills required for VLSI systems design in the nanometre era
- illustrate the importance of custom design tools and also electronic design automation (EDA) for physical implementation, testing and verifications of VLSI systems

Objectives

As specific objectives, by the end of the course students should be able to:

- be familiar with the modern CMOS fabrication process, physical layout design rules and anticipate trends in VLSI fabrication technologies
- understand the trade-off between the four key design metrics of modern VLSI systems – cost, reliability, speed and power
- recognise the parasitic effect of wires/interconnects and apply wire delay models like lumped RC model and Elmore delay model
- understand the sources of power dissipation and the factors affecting robustness of a VLSI system
- design and optimise multi-level CMOS combinational and sequential circuits using static logic, pass transistor logic and dynamic logic
- operate up-to-date design tools for VLSI systems and evaluate the quality of the outputs (e.g. floorplan, routing, physical layout, etc.)

Content

The module will introduce the design principles of integrated circuit designs with millions of digital devices. It begins with CMOS design flows and fabrication processes that creates modern VLSI and explains the design metrics (performance, power, cost, reliability). The typical combinational and sequential circuit design styles like static logic, pass transistor logic and dynmaic logic will be illustrated with many examples of digital devices. The effect of wires and interconnects on circuit speed and power will be studied. The module will be concluded with a case study of cutting-edge advanced VLSI technologies (e.g. FinFET) and design techniques.

Design Flow and Metrics (1L)

- Design flow: design, synthesis, planning, implementation, fabrication
- Cost: yield and detects of wafer die
- Reliability: noise margins, regenerative property of digital circuits
- Speed: delay definition, Fanout-of-four (FO4) delay
- Power: instantaneous, average, peak

CMOS Fabrication and Layout Design Rules (1L)

- Fabrication process: substrate preparation, photolithography, doping and diffusion, oxidation, packing
- Design rules: micron rules vs scalable rules, CMOS process layers, stick diagrams (sketch)

CMOS Combinational Circuits, Pass Transistor Logic, Dynamic Logic (2L)

- Static complementary CMOS logic, progressive transistor sizing
- Ratioed logic, e.g. pseudo-NMOS
- Pass transistor logic: threshold drop, level restorer, transmission gate
- Dynamic logic: charge leakage, charge sharing, clock feedthrough, backgate coupling, domino logic

Wires and Interconnects (2L)

- Interconnect parameters: capacitance, resistance and inductance
- Wire models: lumped model, lumped RC model, Elmore delay model
- Distributed RC line

Power and Robustness (1L)

- Dynamic power disspation
- Static comsumption
- Power analysis and optimisation technique
- Signal integrity issues

Logical Effort (1L)

- Delay of logic gates
- Derivation of intrinsic delay and logic effort
- Optimisation for buffer sizing and the number of buffer stages
- Branching Effort

I/O and Electrostatic Discharge Protection (1L)

- Input and output (I/O) pad and buffer design
- Tri-state buffers

CMOS Sequential Circuit Design, Clocking (2L)

- Static latches, flip-flops, and registers
- Dynamic designs: C^2MOS register and TSPC latch
- Clock tree and clocking strategies

Advanced VLSI Technology and Design Techniques (e.g. FinFET, 3D stacking) (1L)

- Topics varies every year, *suggestions from students are welcome*.

Coursework

Students are provided with the specification of a custom cell, and a reference design in hardware description language (VHDL), for instance a multiplier-accumulator (MAC) circuit. They will be asked to design the cell using the layout editor and verify its correctness via device extraction and SPICE simulation. The custom cell will then be used in junction with other standard cells in the SKY130 (180nm - 130nm) Process Design Kit (PDK). During the process, they will be instructed to inspect and analyse the generated results and reports from the various design automation tools. Finally, they will verify the final physical layout of the reference design using SPICE simulations.

This activity involves preliminary work (~2h). You are required to read the lab handouts before lab sessions and be familiar with the usage of various design tools for this activity.

A total of 16 hours (including preliminary work) is required to complete this coursework.

Students will have the option to submit a Full Technical Report.

Submission and Assessment

The student will be asked to submit -

- the layout of the custom cell and the extracted SPICE file (25%)
- plots of SPICE simulations that verify the custom cell layout and the reference design (50%)
- a piece of reflective writing on the individual lab experience (25%)

Learning Objectives:

- Gain experience with VLSI/ASIC design tools (e.g. Cadence design tools)
- Learn to create layout for a custom cell design and extract device characteristics for SPICE simulations
- Practise a semi-custom design flow for VLSI/ASIC
- Verify a physical design

Booklists

- (Core) Analysis and design of digital integrated circuits: in deep submicron technology, David A. Hodges, Horace G. Jackson, Resve A. Saleh., 3rd ed, ISBN: 0072283653
- (Recommended) Rabaey, Chandrakasan and Nikolic, Digital Integrated Circuits, 2nd ed, ISBN-13: 978-0130909961
- (Recommended) Weste and Harris, CMOS VLSI Design, 4th ed, ISBN-13: 978-0321547743

Examination Guidelines

Please refer to Form & conduct of the examinations [2].

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