ENGINEERING TRIPOS PART IA

Monday 10 June 2013 9 to 12

Paper 3

ELECTRICAL AND INFORMATION ENGINEERING - SOLUTIONS

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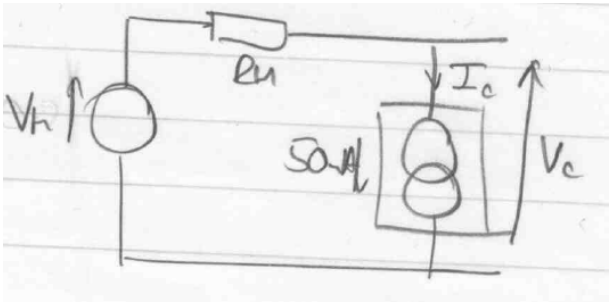
Section C: Dr S Hofmann

SECTION A

1 **(long)**

(a) Convert everything to the left of the camera into a Thevenin equivalent circuit:



$$R_{th} = \frac{6 \times 3}{6 + 3} + 2 + 2 = 6\ \Omega$$
$$V_{th} = \frac{6}{6 + 3} \times 0.9 = 0.6\ \text{V}$$

Hence, we can find the potential difference across the camera from the new circuit (above) to be

$$V_c = V_{th} - I_c R_{th} = 0.6 - 0.05 \times 6 = \boxed{0.3\ \text{V}}$$

Let the voltage across the 6 Ω resistor be V'. Now

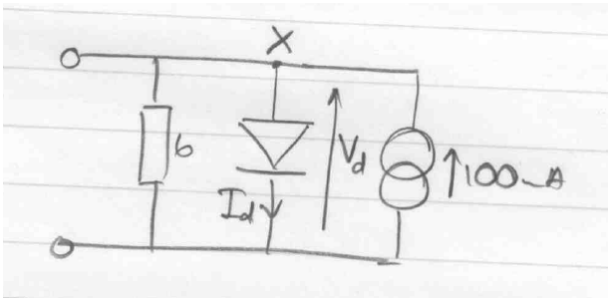
$$V' = V_c + 4I_c = 0.03 + 4 \times 0.05 = 0.5\ V$$

Hence,

$$I_b = \frac{V_b - V'}{3} = \frac{0.9 - 0.5}{3} = \boxed{133\ \text{mA}}$$

NOTE: You cannot use the Thevenin equivalent circuit to determine I_b, as the theorem only says that the Thevenin circuit appears equivalent to the original circuit to anything *outside* the equivalent circuit.

(b)

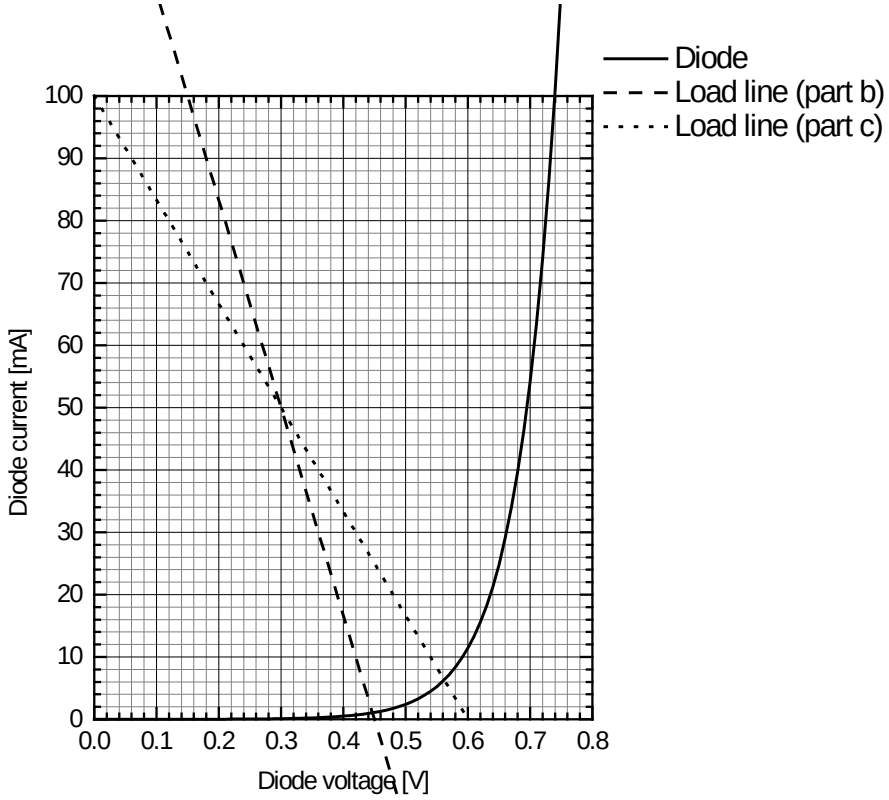


We need a relation between V_d and I_d to plot on the diode graph (this will be our load line). This can be achieved by performing a nodal voltage analysis at point X,

$$\sum I_{out} = 0 = -0.1 + I_d + \frac{V_d}{6}$$

$$\therefore I_d = 0.1 - \frac{V_d}{6}$$

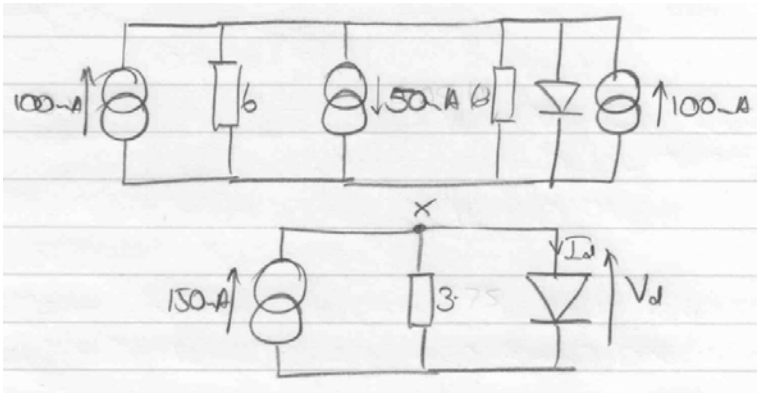
We plot this line on the graph.



From the intersection of the two lines, we have the operating point, giving

$V_o = \boxed{0.56\text{ V}}$

(c) We need a new operating point for the cell, so we put the two circuits together and simplify using Norton and Thevenin:



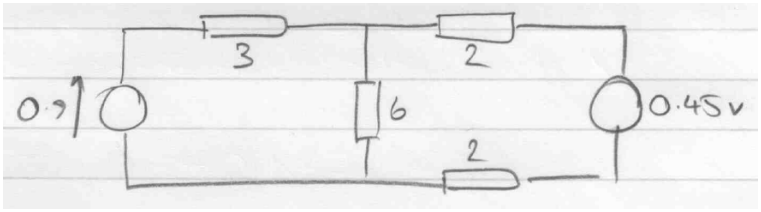
Performing a Nodal Voltage Analysis at X:

$$\sum I_{out} = 0 = -0.15 + I_d + \frac{V_d}{3}$$
$$\therefore I_d = 0.15 - \frac{V_d}{3}$$

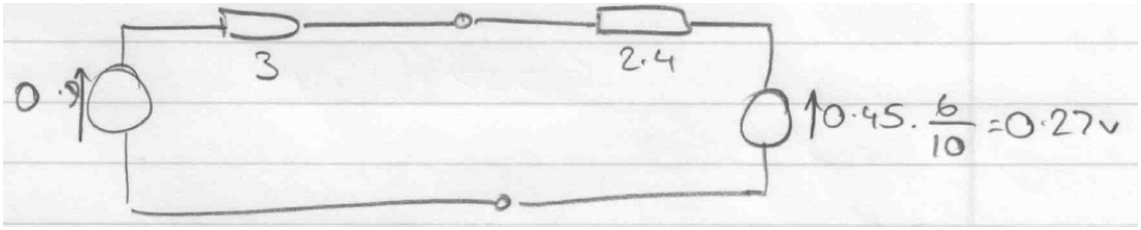
We now plot the new load line on the diode characteristics (also shown on the previous page), and from the operating point, we have

$V_o = \boxed{0.45\text{ V}}$

To calculate the new battery current, I_b, we must again return to the original circuit for the battery itself. However, we now know that the diode has a fixed voltage of 0.45 V between its terminals, so we can treat this like a fixed voltage source of this value. Hence, out circuit effectively becomes



Converting the right hand side to a Thevenin equivalent (taking care not to convert the battery!) gives



Hence, we can find the battery current to be

$$I_b = \frac{0.9 - 0.45}{3 + 2.4} = \boxed{83\text{ mA}}$$

Therefore, the solar cell has acted to reduce the current drawn from the battery, which should prolong the time before it needs to be replaced (although the question does not ask you to state this!)

2 **(long)**

(a) We can gain the power factor of the factory from the power consumed, the voltage supplied and the current drawn as

$$\cos\phi = \frac{P}{VI} = \frac{30000}{240 \times 147} = \boxed{0.85}$$

(b) To get the real power dissipated in the line, we need to calculate the current, I_l, on the high voltage side of the step-down transformer, using the turns ratio, which in turn is given by the ratio of the voltages on the high and low voltage sides

$$I_l = \frac{240}{10000} \times 147 = 3.528 \text{ A}$$

Knowing the resistance of the line, we can calculate the power dissipation from

$$P_{line} = I_l^2 R_{line} = 3.528^2 \times 100 = \boxed{1245 \text{ W}}$$

(c) There are two basic methods for calculating the voltage at the power station. One is to calculate the voltage drop across the transmission line, and then add this to the voltage drop across the tow. However, to do this you need to remember that the transmission line voltage will be out of phase with that across the factory, as the current in the transmission line (and town) is out of phase with the voltage across the factory. It is therefore *much* easier to use conservation of real and reactive power. We already know the real power in the factory and transmission line, but we need to calculate the reactive power in both the factory and transmission line, which is

$$Q_{line} = I_l^2 X_{line} = 3.528 \times 100 = 1245 \text{ VAR}$$
$$Q_{fact} = P_{fact} \tan\phi = 30000 \tan(\cos^{-1} 0.85) = 18600 \text{ VAR}$$

Hence, the total apparent power output from the power station is

$$S_{tot} = \sqrt{\left(P_{fact} + P_{line}\right)^2 + \left(Q_{fact} + Q_{line}\right)^2}$$
$$S_{tot} = \sqrt{(30000 + 1245)^2 + (18600 + 1245)^2}$$
$$S_{tot} = 37.0 \text{ kVAR}$$

Hence, the voltage at the power station is

$$V_p = \frac{S_{tot}}{I_l} = \frac{37000}{3.528} = \boxed{10.5\text{ kV}}$$

(d) (i) We need a capacitor to generate 18600 VAR to compensate Q_{fact}. Hence,

$$-Q_c = \frac{V^2}{X_c} = -\omega C V^2$$
$$\therefore C = \frac{Q_{fact}}{2\pi f V^2} = \frac{18600}{2\pi \times 50 \times 240^2} = \boxed{1.03\text{ mF}}$$

(ii) To calculate the new power dissipation in the transmission line, we need the new current in the factory which, given the power factor is now unity, is

$$I = \frac{P}{V} = \frac{30000}{240} = 125\text{ A}$$

The line current is then

$$I_l = \frac{240}{10000} \times 125 = 3\text{ A}$$

So the power dissipated in the line has dropped to

$$P_{line} = I_l^2 R_{line} = 3^2 \times 100 = \boxed{900\text{ W}}$$

(iii) To determine the impedance seen by the factory, we need the actual impedance of the factory first, R_{fact}. As we have corrected the power factor of the factory to unity, we know that the factory presents a purely resistive load of

$$R_{fact} = \frac{V^2}{P} = \frac{240^2}{30000} = 1.92\ \Omega$$

We now refer this load to the primary side of the transformer using square of the turns ratio

$$R'_{fact} = \left(\frac{n_1}{n_2}\right)^2 R_{fact} = \left(\frac{10000}{240}\right)^2 1.92 = 3333\ \Omega$$

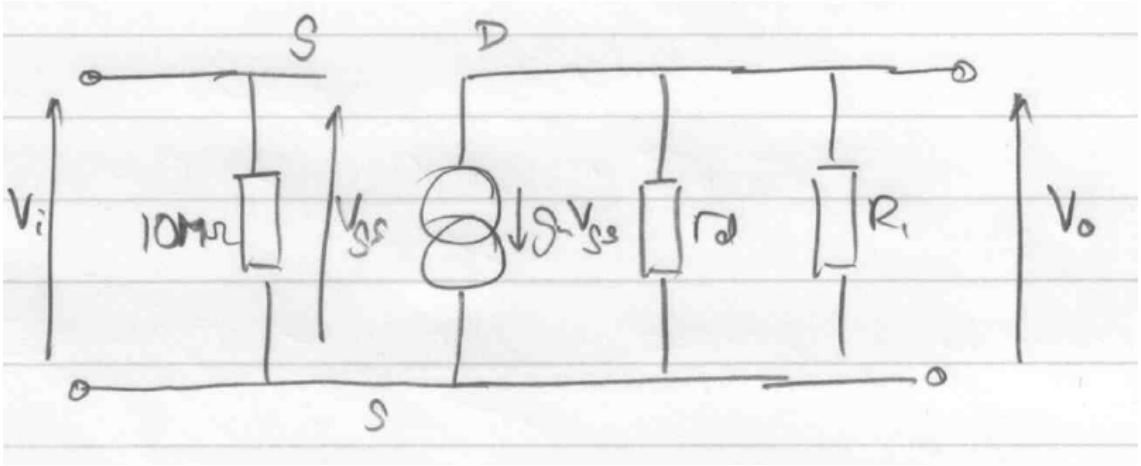
We add this to the impedance of the transmission line to give the total impedance seen by the power station

$$Z_{tot} = \boxed{(3433 + 100\text{j})\ \Omega}$$

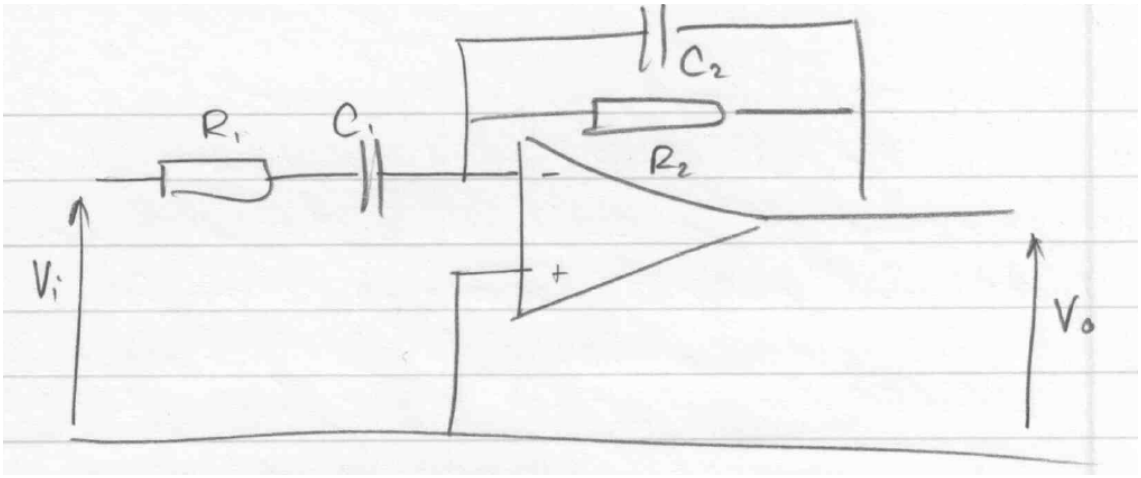
3 **(short)**

(a) Capacitors C_1 and C_3 are coupling capacitors. C_1 removes any d.c. component from V_i which would otherwise affect the operating point of the amplifier. C_3 removes the d.c. component due to the operating point from V_o. C_2 is a bypass capacitor which increases circuit gain by removing a.c. feedback which would otherwise be generated by the presence of the self-biasing resistor R_2.

(b)



4 **(short)** This circuit is required to have a negative gain, and a well-defined input resistance which is not infinite. Therefore, an inverting amplifier circuit should be used with the addition of a capacitor in series with the input resistor to give a low frequency cut-off and a capacitor in parallel with the feedback resistor to give a high frequency cut-off. The circuit will therefore be



To fix the input resistance at 1 kΩ, we will require

$R_1 = \boxed{1\ \text{k}\Omega}$

To fix the gain, *G*, at –15,

$$G = \frac{-R_2}{R_1}$$
$$\therefore R_2 = -R_1 G = -1000 \times -15 = \boxed{15\ \text{k}\Omega}$$

C_1 and R_1 together fix the low frequency cut-off when

$$R_1 = \frac{1}{\omega_c C_1}$$
$$\therefore C_1 = \frac{1}{\omega_c R_1} = \frac{1}{2\pi \times 20 \times 1000} = \boxed{7.96\ \mu\text{F}}$$

C_2 and R_2 together fix the high frequency cut-off when

$$R_2 = \frac{1}{\omega_c C_2}$$

$$\therefore C_2 = \frac{1}{\omega_c R_2} = \frac{1}{2\pi \times 20000 \times 15000} = \boxed{530 \text{ pF}}$$

5 **(short)**

(a) The circuit will oscillate at the frequency when there is perfect energy transfer between the inductor and capacitor, which will occur when their reactances are equal and opposite to each other. Current is oscillating in the circuit.

(b) From the Data Book, we know that the Q-factor is related to bandwidth and resonant frequency by

$$Q = \frac{f_0}{\Delta f} = \frac{1.026 \times 10^6}{5 \times 10^3} = 205.2$$

We can also relate the Q-factor to the total resistance in the circuit (using the equation in the Data Book)

$$R_{tot} = \frac{\omega_0 L}{Q} = \frac{2\pi \times 1.026 \times 10^6 \times 10 \times 10^{-3}}{205.2} = 314\ \Omega$$

However, there is already a 100 W series resistance in the circuit, so the additional resistance required is

$$R = R_{tot} - 100 = \boxed{214\ \Omega}$$

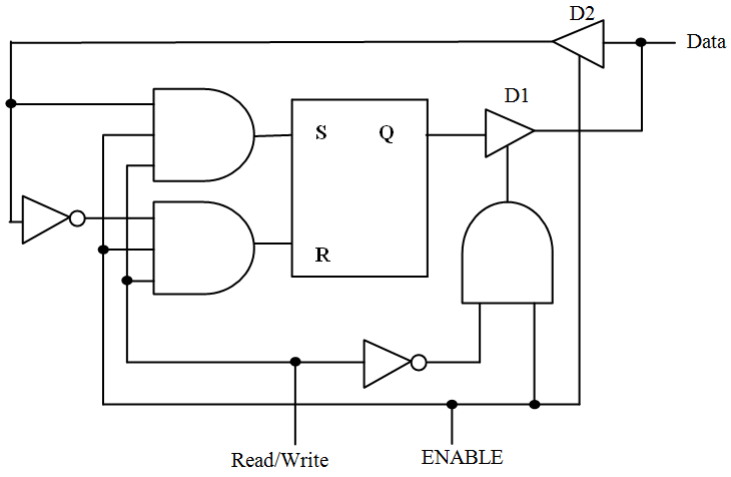
SECTION B

6 (a) **Data bus:** Parallel electrical connections (two ways) through which the microprocessor exchanges data with the memory (read or write). In this case there are 8 such connections. **Address bus:** Parallel connections (one way from the microprocessor to the memory) used to select locations in the memory from which the data is to be obtained or stored.

(b) The number of bistables = number of bits in the memory. 14 bits address bus results in 2^{14} memory locations each of 8 bits. That means that number of bits is 2^{14} x 2^3 = 2^{17} bits (bistables). 1 kbyte =1020 bytes = 2^{10} bytes = 2^{13} bits (as 1 byte = 8 bits). The capacity = total number of bistables in each integrated memory chip= 2^{17} bits = =2x2^{10} x 2^3 bytes = 16 kbytes.

(c) The circuit below is a one-bit memory. The D1 and D2 are active buffers (repeat the signal) when the control terminal is at '1' and act as 'open circuit' when the control terminal is at '0'. That means when Y=ENABLE is at '0' the X=Data is isolated from the memory chip (as D1 and D2 are both in 'open circuit).

- When ENABLE =1 and Z/W=Read/Write =1 (indicating write) then D1 has the control terminal at 0, meaning that is in open circuit while D2 will be active allowing SET (S) /RESET (R) to be set to 1/0 if the data is 1 or 0/1 if the data is 0. In other words the 'data' is 'written' as Q – the state of the bistable.
- When ENABLE =1 and Z/W=Read/Write =0 (indicating read) then D1 will be active allowing Q to be transferred out as Data (Data =Q). D2 is in open circuit, not allowing the data to be written in the bistable.



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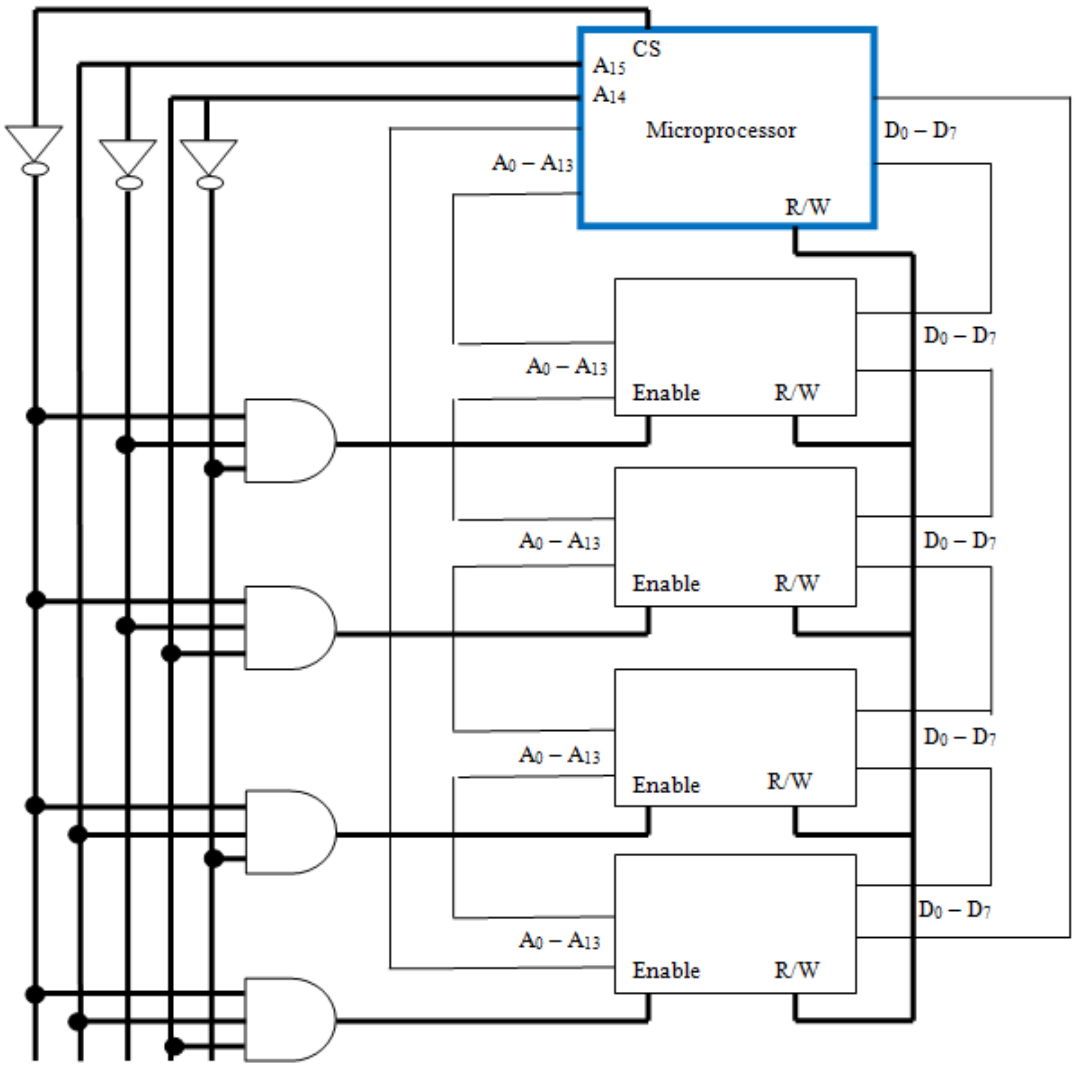
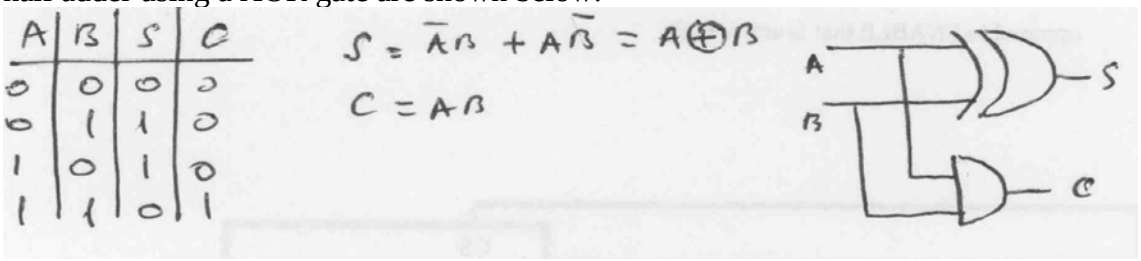
(d) The memory has 14 bit address bus while the microprocessor has 16 bits address bus. This means that $2^2 = 4$ integrated memory chips could be connected to the microprocessor. Note that CS' is active low as opposed to ENABLE that is active high.

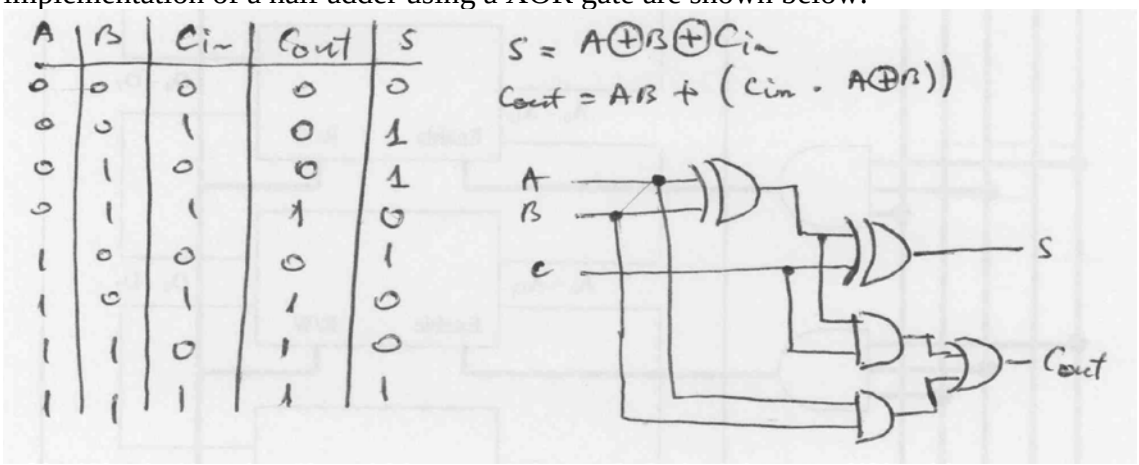


7 **(short)**

(a) Half adder. The logic table, logic expression and the implementation of a half adder using a XOR gate are shown below:

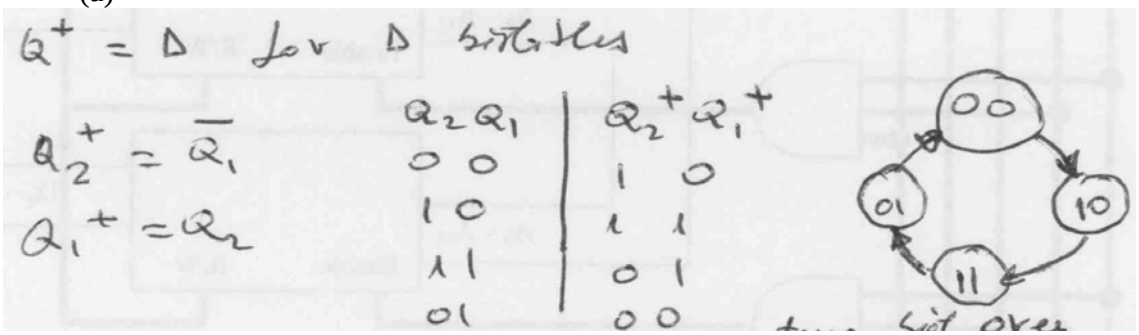


(b) (b) The full adder. The logic table, logic expression and the implementation of a half adder using a XOR gate are shown below:



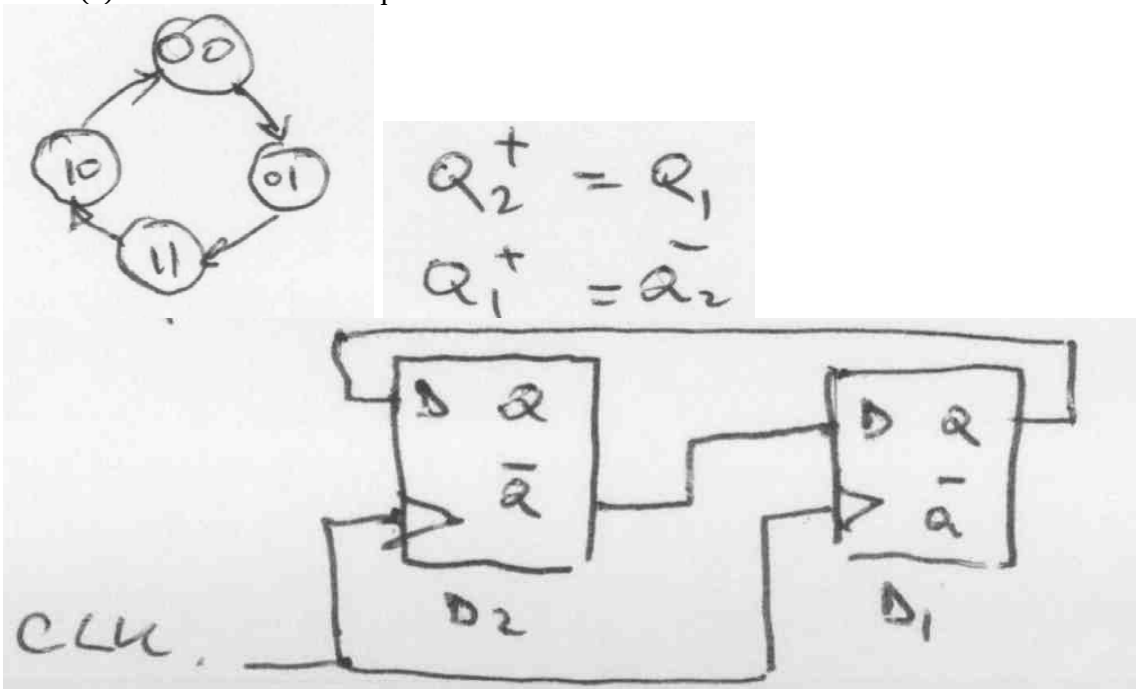
8 **(short)**

(a)



(b) This is a Grey code, in which only one bit changes at a time. It is used in sequential logic applications where dynamic hazards must be avoided

(c) To reverse the sequence



9 **(short)**

(a) This is a weighted-resistor DAC. With the op-amp ideal, the inverting terminal is at virtual ground. Voltages across S_0 to S_3 contribute currents to the summing junction in inverse proportion to the value of each of the resistances. Hence the contribution to the output voltage V_0 is also in inverse proportion to the resistances (R, 2R, 4R and 8R). S_o is therefore the LSB and S_3 the MSB.

The sources need to be Thevenin voltages capable of being switched on and off (under the control of a digital circuit). Typically MOS transistors can be used for this.

(b) Since the inverting input of the op-amp is virtual earth, the input resistance at the terminal S_2 is R_{in2}=2kΩ and the input resistance at the terminal S_1 is R_{in1}=4kΩ

(c) The output voltage $V_0 = -R/2\ [S_o/8R + S_1/4R + S_2/2R + S_3/R]$
Since a '1' digital is 5 V in analogue. It means $S_o = S_1 = S_3 = 5V$ while $S_2 = 0V$.
That means:
$V_0 = -5/2\ [1/8+1/4 +1]=-3.4375$ V

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SECTION C

10 **(short)**

(a) Based on l>> solenoid radius, magnetic flux density inside the solenoid can be assumed to be uniform.

Ampere's law: circulation of B = μ_0 × current enclosed

hence $$B \times l = \mu_0 \times N \times I$$

(for rectangular Amperian path of length l through

so $$B = \mu_0 \times \frac{N}{l} \times I$$

(b) Magnetic flux through 1 turn: $\Phi = B \times A$

Flux linked for N turns: $$\Phi' = N \times B \times A = \frac{\mu_0 \times N^2 \times A}{l} \times I$$

Self inductance $$L = \frac{\Phi'}{I} = \frac{\mu_0 \times N^2 \times A}{l}$$

for the given values: $$L = \frac{\mu_0 \times 300^2 \times (4 \times 10^{-4} m^2)}{0.25m} = 181 \mu H$$

(c) $$emf = -L \times \frac{dI}{dt} = -(181 \times 10^{-6} H) \times (50 A/s) = 9.05 mV$$

11 **(short)**

(a) (i) The capacitor filled with the slab of dielectric material is equivalent to two parallel-plate capacitors of the area A connected in series, one with plate separation d/3 (with ε_r=3) and the other with plate separation 2d/3 (with ε_r=1).

Hence $$\frac{1}{C}=\frac{1}{C_1}+\frac{1}{C_2}=\frac{d/3}{\varepsilon_r\varepsilon_0 A}+\frac{2d/3}{\varepsilon_0 A}$$

and $$C=\frac{3\varepsilon_r}{2\varepsilon_r+1}\times C_0=\frac{9}{7}C_0$$

so ratio is 9/7

(ii) Charges on induced on one side of the metal slab must be opposite and equal to other side, ie the net charge on metal slab remains 0. Hence the capacitor filled with the metal slab is equivalent to two parallel-plate capacitors of the area A connected in series, each having a plate separation of d/3.

Hence $$C=\frac{\varepsilon_0 A}{2d/3}=1.5C_0$$

so ratio is 1.5

(b) For charged capacitor with dielectric:

$$C=\frac{Q}{V_1}=\frac{2\varepsilon_0 A}{d}$$

when dielectric is removed, charge on the capacitor remains the same:

$$V_{air}=\frac{d}{\varepsilon_0 A}Q=2V_1=100V$$

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12 **(long)**

(a) The cross-sectional area of the outer conductor is

$$A = \pi(c^2 - b^2)$$

and the resistance is given by

$$R = \frac{\rho_c L}{A} = \frac{\rho_c L}{\pi(c^2 - b^2)}$$

(b) (i) Use Ampere's law, currents are opposite equal, hence B=0 for r>c

(ii) Use Ampere's law: circulation of B = μ_0 × current enclosed

$$B \times 2\pi r' = \int JdA = \int (\alpha r')(2\pi r' dr')$$

for r<a: the enclosed current is

$$I_{enc} = \int_0^r 2\pi\alpha r'^2 dr' = \frac{2\pi\alpha r^3}{3}$$

hence

$$B_1(2\pi r) = \frac{2\mu_0\pi\alpha r^3}{3}$$

so

$$B_1 = \frac{\mu_0\alpha}{3} r^2$$

(iii) for a<r<b: the enclosed current is

$$I_{enc} = \int_0^a 2\pi\alpha r'^2 dr' = \frac{2\pi\alpha a^3}{3}$$

hence

$$B_2(2\pi r) = \frac{2\mu_0\pi\alpha a^3}{3}$$

so

$$B_2 = \frac{\mu_0\alpha a^3}{3r}$$

(c) Consider a differential element which is made up of thin cylinder of inner radius r and outer radius r+dr and length L. Its contribution to the resistance is given by

$$dR = \frac{\rho_D dl}{A} = \frac{\rho_D dr}{2\pi rL}$$

where A=2πrL is the area normal to the direction of current flow. The total resistance of the coaxial dielectric becomes:

$$R = \int_a^b \frac{\rho_D dr}{2\pi rL} = \frac{\rho_D}{2\pi L} \ln(\frac{b}{a})$$

ENGINEERING TRIPOS PART IA

Monday 10 June 2013 9 to 12

Paper 3

ELECTRICAL AND INFORMATION ENGINEERING

NUMERICAL SOLUTIONS

1 (a) 0.3 V, 133 mA
(b) 0.56 V
(c) 0.45 V
(d) 116 mA

2 (a) 0.85
(b) 1245 W
(c) 10.45 kV
(d) (i) 1.03 mF
(ii) 900 W
(iii) (3433+100j) Ω

5 (b) 214 Ω

6 (b) 16 kbytes

9 (c) -3.4375 V

10 (b) 181 μH
(c) 9.05 mV

11 (a) (i) 9/7
(ii) 3/2
(b) 100 V

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