Engineering Tripos, Part IA, 2022

Paper 3 Electrical and Information Engineering

Solutions

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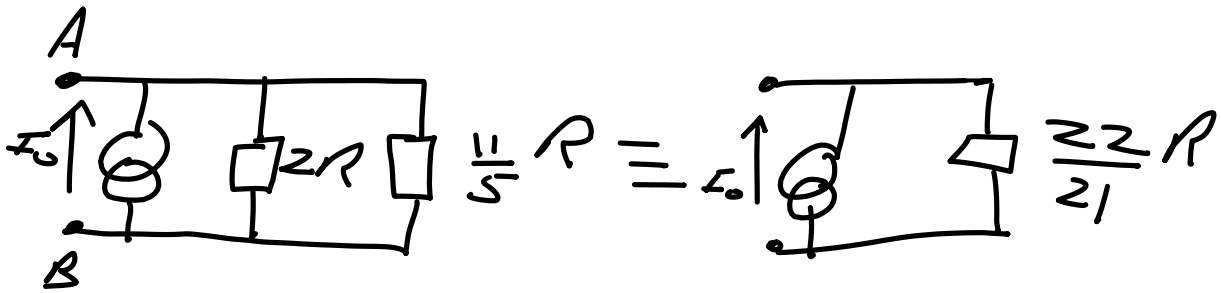
SECTION A

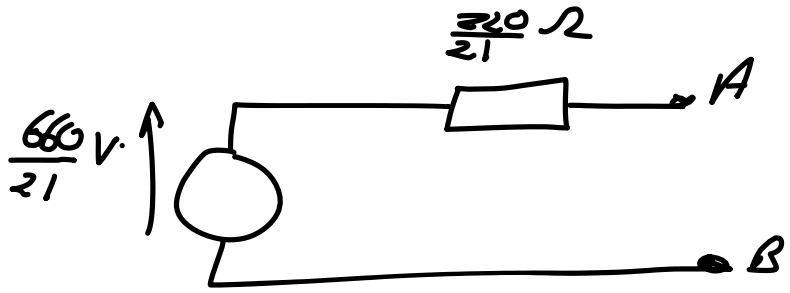
1. (short)

(a) Reducing the loops across AB starting from the outermost one, we end up with

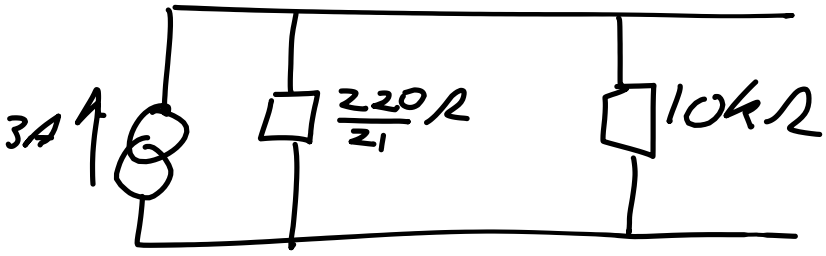


Is the equivalent impedance across the I_O current source. The short circuit current remains I_O. The Norton equivalent across AB is therefore the I_O in parallel with an impedance 22/21 R

(b)



(c)



The power dissipated in the whole system is given by I^2r, where r is the complete resistance, given by 220/21 || 10^4 W. This has the numerical value 10.46 W.

Therefore, $P = I^2$x10.46 = 94.14 W

2. (short)

(a) The open circuit voltage gain (amplification) = A

(b) With a resistor R connected across BC

$$V_{BC} = \frac{R}{R + R_{OUT}} . AV_{in}$$

Therefore amplification

$$\frac{V_{BC}}{V_{in}} = \frac{AR}{R + R_{OUT}}$$

(c) Power output

With $R = R_{OUT}$

$$P_{BC} = \frac{A^2 V_{in}^2}{4R_{OUT}} = P_{OUT} \quad P_{IN} = \frac{V_{in}^2}{R_{in}} \quad power\ gain = \frac{P_{OUT}}{P_{IN}} = \frac{R_{in} A^2}{4R_{OUT}}$$

(d) With

$$P_{BC} = \frac{V_{BC}^2}{R} = \frac{RA^2 V_{in}^2}{(R + R_{OUT})^2}$$

$$\frac{dP_{BC}}{dR} = \frac{A^2 V_{in}^2}{(R + R_{OUT})^2} - \frac{2RA^2 V_{in}^2}{(R + R_{OUT})^3}$$

$$\frac{dP_{BC}}{dR} = 0 \quad \therefore \ R + R_{OUT} = 2R \ \ R = R_{OUT}$$

Is the condition for maximum power output.

3. (long)

(a) For the potential divider on the Gate, as we know R_1 = 4.25 MW, we must therefore have R_2 = 0.75 MW.

The drain bias resistor, R_3 from the operating point is calculated as 1.25 KΩ.

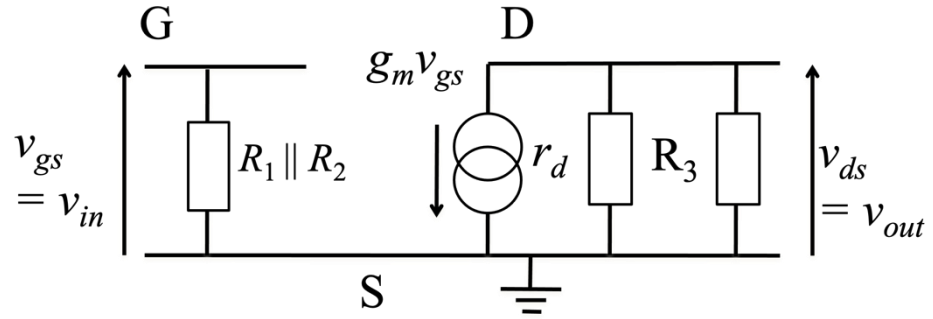
(b) The small signal equivalent circuit parameters are determined by considering the linearised input to output variations at the operating point.

$$\frac{\partial i_d}{\partial v_{gs}} = g_m \ and \ \frac{\partial i_d}{\partial v_{ds}} = \frac{1}{r_d}$$

From Fig 3a, for the operating point at $V_{GS} = 3\ V$

$$\frac{\Delta i_d}{\Delta v_{gs}} = \frac{4\ mA}{1\ V} = 4.0x10^{-3}\ S = \ g_m$$

(c)



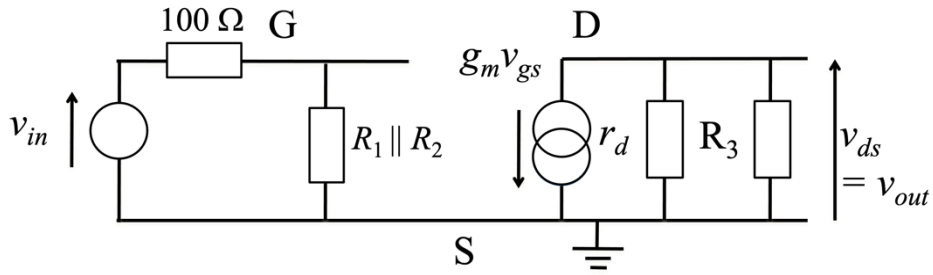
(d) The input resistance is $R_1||R_2$ = 637.5 kW

The output resistance is $r_d||R_3$ = 1.11 kW

Using the small signal equivalent circuit $v_{in} = v_{gs}$

We have $v_{out} = -g_m v_{gs} \frac{R_3 r_d}{R_3 + r_d} = \ 4x10^{-3} v_{gs} \frac{1\times12.5\times10^6}{11.25\times10^3} = \ -4.44 v_{gs}$

(e)



The proportion of v_{in} which now gets dropped across the gate is reduced in proportion to the ratio of ($R_1||R_2$) to the 100 W resistance.

This means that of the 400 mV input, only 400 × 1111/1211 = 367 mV reaches the gate.

Therefore, the output will be correspondingly smaller by the same factor, and this is the factor by which the gain will be reduced.

i.e. the output voltage = -400×4.44×(1111/1211) = -1.631 V.

4. (short)

(a) Turns ratio of transformer. From open circuit test

$$\frac{\tilde{V}_{IN}}{\tilde{V}_{OUT}} = \frac{11\ kV}{66\ kV} = \frac{1}{6} \quad \therefore \ n = 1:6$$

(b)

The R_0 term in the equivalent circuit represents the hysteresis and eddy current losses. It is determined from the open-circuit test.

$$\frac{\tilde{V}_{IN}}{R_O} = 0.1\ x\ 0.8\ A \quad R_O = \frac{11x\ 10^3}{8\ x\ 10^{-2}} \quad Losses\ are\ the\ power\ disspated\ in\ R_O = \frac{\tilde{V}_{in}^2}{R_O} = 880\ W$$

(c) The magnetising reactance is X_O in the equivalent circuit. From open circuit test

$$\frac{\tilde{V}_{IN}}{0.1\ x\ \sin(\cos^{-1} 0.8\ )} = \frac{11\ x10^3}{0.1\ x\ 0.6} = 183.3\ k\Omega$$

X_T represents the leakage reactance. From short circuit test

$$\tilde{V}_{IN} = \tilde{I}_{IN}.R_T + j\ \tilde{I}_{IN}\ X_T$$

From the power measurement

$$\left|\tilde{I}_{IN}\right|^2 R_T = 270\ W \quad \therefore \ R_T = 30\ \Omega \quad and \ \left|\tilde{V}_{IN}^2\right| - \left|\tilde{I}_{IN}^2 R_T^2\right| = \left|\tilde{I}_{IN}^2 X_T^2\right| = 25\ x\ 10^4 - 81x\ 10^2 = 2.419x\ 10^5 \quad \therefore \quad X_T X_T = \frac{\sqrt{2.419\ x\ 10^5}}{3} = 163.9\ \text{W}$$

In an ideal transformer, X_T would be zero (no leakage flux) and X_O infinite and there would be no losses in the core.

5. (long)

(a) If the Op Amp is considered in negative feedback mode then we can assume (i) both terminals are at the same potential and (ii) no current is drawn into the terminals. Therefore, the voltage across R_1 is the same as v_{in}.

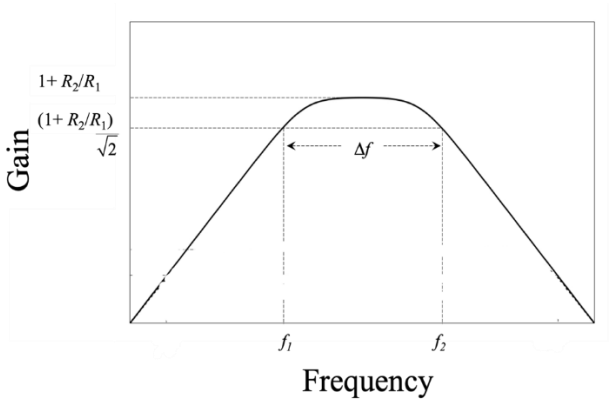
i.e. $v_{in} = v_{out}\frac{R_1}{R_1+R_2} \implies \frac{v_{out}}{v_{in}} = \frac{R_1+R_2}{R_1} = 1 + \frac{R_2}{R_1}$

(b) This will be similar to before but R_1 and R_2 will be replaced by Z_1 and Z_2 respectively,

where $Z_2 = \frac{R_2}{1+j\omega C_2 R_2}$ and $Z_1 = R_1 + \frac{1}{j\omega C_1}$

This leads to a gain of:

$$\frac{v_{out}}{v_{in}} = 1 + \frac{Z_2}{Z_1} = 1 + \frac{R_2}{R_1} \times \frac{1}{1 + j\omega C_2 R_2} \times \frac{1}{1 + \frac{1}{j\omega C_1 R_1}}$$



(c) To get a gain of 10, R_2 = 45 kΩ and R_1 = 5 kΩ.

The upper -3 dB frequency is given by the term 1 + jwC_1R_1, and occurs at $f_2 = 1/(2\pi R_2C_2)$. Given that f_2 = 10 MHz, this implies $C_2 = 1/(2\pi \times 45 \times 10^3 \times 10^6) = 3.5$ pF

The lower -3 dB frequency is given by the term 1 + $1/jwC_1R_1$, and occurs at $f_1 = 1/(2\pi R_1C_1)$. Given that f_1 = 100 Hz, this implies $C_1 = 1/(2\pi \times 5 \times 10^3 \times 100) = 3.18$ nF

(d). When an inductor is added, there will be a resonance peak at an angular frequency $\omega_0 = \frac{1}{\sqrt{LC}}$

SECTION B

6 (short)

(a) (i) 64 kbits = 2^{16} bits, 4 data lines = 2^2

Hence $2^{(16-2)} = 2^{14}$ locations => 14 address lines.

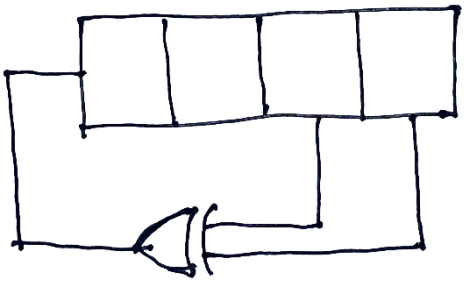
Therefore, the connections are 4 data lines, 14 address lines, $\overline{CS}$ for chip select and R/$\overline{W}$ for read but not write.

(ii) 64 kbytes = 64 k × 2^3 bits = 2^{19} bits.

Hence $2^{19} / 2^{16} = 2^3 = 8$ devices.

(b) (i) A shift register is a type of sequential logic circuit where a set of storage elements arranged in series. They share a single clock signal, which causes the data stored in the system to shift from one location to the next, with the $(N+1)^{th}$ bistable takes in the value of the N^{th} from the one before.

(ii)



Sequence: 0000

1111
0111
0011
0001
1000
0100
0010
1001
1100
0110
0101
1010
1101
1110

15 long sequence. This is the longest.

7 (short)

(a)

	Operation	**Clock cycle**
movlw 0x31;	Moves 0x31 into W;	1
movwf FSR;	Moves (address) 0x31 into FSR; [to set up indirect addressing]	1
call sr;	Call subroutine labelled sr;	2
decf FSR;	Decrements FSR; [now pointing to 0x30]	1
call sr;	Call subroutine;	2
sleep;	Ends program;	1
……		
sr rrf INDF;	Rotates right FRS contents; [effectively ÷2]	1
movlw 0x10;	Move 0x10 to W;	1
addwf INDF;	Add 10 to contents of FSR; [i.e. original numb/2 + 16 (decimal)]	1
return;	Return to main program;	2

(b) Contents of 0x30 = 20/2 +16 = 26 (0x1A)
Contents of 0x31 = 50/2 +16 = 41 (0x29)
Contents of W = 16 (0x10) as last time, changed in the 2nd call of subroutine.

(c) Clock = 20 MHz => 1 cycle = 1 period = $1/(20\text{x}10^6)$ = 50 ns
Main program 8 cycles
Subroutine 5 cycles
Subroutine called twice
=> Total number of clock cycles = 8 + (2x5) cycles = 18 cycles
Total run time = 18 x 50 ns = 900 ns

8 (short)

(a) This is a weighted-resistor DAC. With the op-amp ideal, the inverting terminal is at virtual ground. Voltages across S_0 to S_3 contribute currents to the summing junction in inverse proportion to the value of each of the resistances. Hence the contribution to the output voltage V_0 is also in inverse proportion to the resistances (R, 2R, 4R and 8R). S_0 is therefore the LSB and S_3 the MSB.

(b) Since the inverting input of the op-amp is virtual earth, the input resistance at the terminal S_2 is R_{in2} = 2 kΩ and the input resistance at the terminal S_1 is R_{in1} = 4 kΩ.

(c) The output voltage $V_0 = -R/2\ [S_0/8R + S_1/4R + S_2/2R + S_3/R]$. Since a "1" digital is 5 V in analogue. It means $S_0 = S_1 = S_3 = 5V$ while $S_2 = 0$ V.

That means: $V_0 = -5/2\ [1/8+1/4 +1]=-3.4375$ V

9 (long)

(a) Main characteristics:

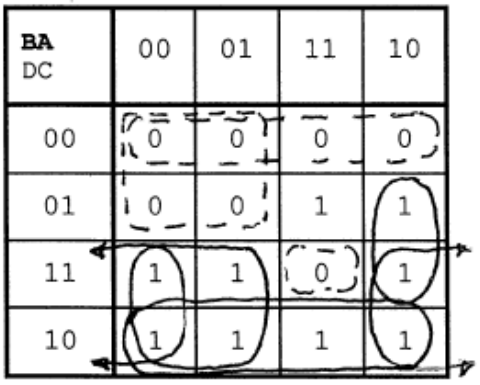
- In combinational logic, the state of the outputs is governed only by the present state of the inputs.
- In sequential logic, the state of the outputs is affected not only by the present state of the inputs, but also by their previous state.
- Sequential logic typically contains bi-stables or memory elements in which "states" or "results" can be stored.
- Sequential logic can often be created by rearranging the connections to combinational logic in such a way as to cause feedback.

(b) Construct a truth table:

Input				Output
D	C	B	A	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1

Input				Output
D	C	B	A	Y
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

and map the expression:



(i) For the NAND solution, encircle groups of 1s (or 0s), as shown, to deduce the minimum number of terms. Considering the 1s, we get the expression:

$Y = D \cdot \bar{C} + D \cdot \bar{B} + D \cdot \bar{A} + \bar{D} \cdot C \cdot B$ which satisfies the requirements.
Note that no attempt has yet been made to eliminate static hazards.
This can be simplified: $Y = D \cdot (\bar{C} + \bar{B} + \bar{A}) + \bar{D} \cdot C \cdot B$ and rewritten using De Morgan:
$Y = \overline{\overline{D \cdot \bar{C}} \cdot \overline{D \cdot \bar{B}} \cdot \overline{D \cdot \bar{A}} \cdot \overline{\bar{D} \cdot C \cdot B}}$, using two, three and four input NANDs.

(ii) For the NOR solution, consider the encircled 0s (to get $\bar{Y}$), and apply De Morgan to the result:

$Y = \bar{C} \cdot \bar{D} + \bar{B} \cdot \bar{D} + A \cdot B \cdot C \cdot D = (\overline{D + C}) + (\overline{B + D}) + (\overline{\bar{A} + \bar{B} + \bar{C} + \bar{D}})$
Hence we get: $Y = \overline{\overline{D + C} + \overline{B \cdot D} + \overline{\bar{A} + \bar{B} + \bar{C} + \bar{D}}}$, using two, three and four input NOR gates.

(c) Static hazards can be detected in the Karnaugh map by identifying regions which touch but do not intersect. They can be overcome by summing additional product terms which intersect the touching region or regions. In the present case, the additional term $C \cdot B \cdot \bar{A}$ can be incorporated to counter the static hazard arising from touching terms $\bar{D} \cdot C \cdot B$ and $D \cdot \bar{A}$.

(d) The Karnaugh map technique is effective for minimising Sum of Product expressions, provided;

- both 1s and 0s are considered when drawing loops, and
- only a single output is required.

There is no simple way of identifying the economies that might arise if more than one output is to be generated, some of which may be able to share common terms. Also, it may be possible to find a more economical solution using fewer packages in ways not directly deduced from the map. For example, cells which are adjacent along a diagonal are related by the XOR of two input variables; use of an XOR gate can thus offer possible economies.

SECTION C

10 (short)

(a) Since $D = \frac{\rho}{2\pi r} = \frac{Q}{2\pi rL}$,

$$V = \frac{Q}{2\pi\varepsilon_o\varepsilon_r L} In(\frac{R_1}{R_2})$$

Thus we can have Q=2.49×10^{-6} C as the charge on the inner conductor.

(b) Capacitance of the coaxial cable:

$$\text{Since } Q = CV$$

$$C = \frac{Q}{V} = 4.98 \times 10^{-7}\ F = 0.498\ \mu F$$

11 (short)

(a) The magnetic flux density at the central of the two parallel wires B = B_1+B_2

$$B_i = \frac{\mu_o I_i}{2\pi a}$$

$$a = \frac{l}{2} = 20cm$$

$$B = B_1 + B_2 = \frac{\mu_o I_1}{2\pi a} + \frac{\mu_o I_2}{2\pi a} = 4 \times 10^{-5} T$$

The direction is out of the paper.

(b) The magnetic flux

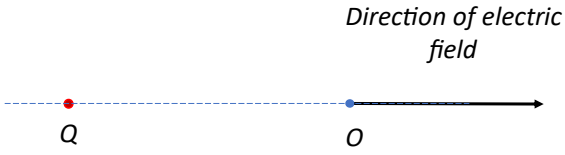
$$\Phi = \int_{L_1}^{l-L_2} (B_1 + B_2) d\, dr = \int_{L_1}^{l-L_2} (\frac{\mu_o I_1}{2\pi r} + \frac{\mu_o I_2}{2\pi(l-r)}) d\, dr = \frac{\mu_o I_1 d}{2\pi} In3 - \frac{\mu_o I_2 d}{2\pi} In\frac{1}{3}$$

$$= 2.2 \times 10^{-6}\ Wb$$

12 (long)

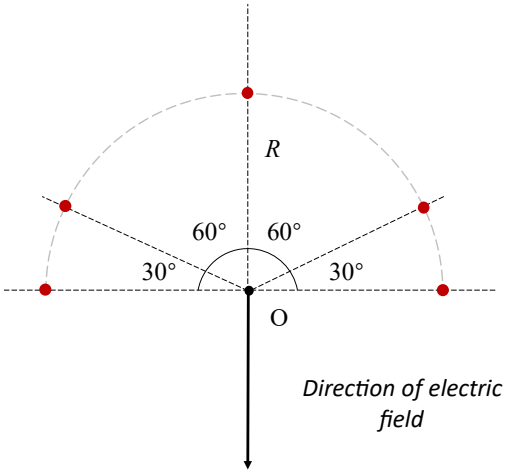
(a) The magnitude and direction of the electric field are:

$$E = \frac{D}{\varepsilon_o} = \frac{Q}{4\pi\varepsilon_o 5^2} = 3.6 \times 10^8 Q \ (\mathrm{V}\ m^{-1})$$

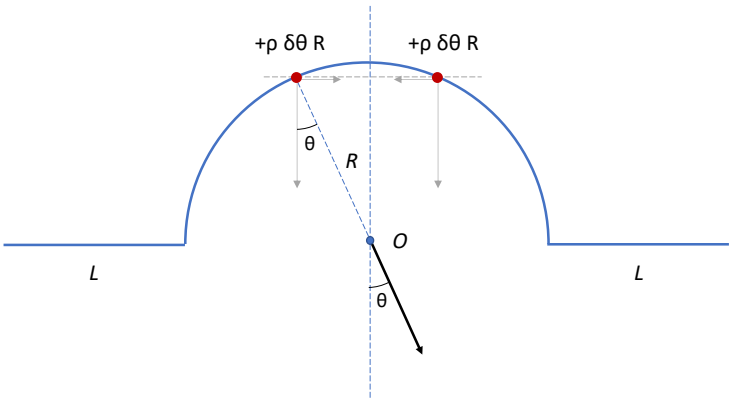


(b) The magnitude and direction of the electric field are:

$$E = \frac{D}{\varepsilon_o} + 2 \times \frac{D}{\varepsilon_o} \times \cos(60°) = 2 \times \frac{Q}{4\pi\varepsilon_o 5^2} = 7.2 \times 10^8 Q \ (\mathrm{V}\ m^{-1})$$



(c) Since the two straight sections are symmetrical with regards to the point O (centre of the semicircle), therefore their electrical filed cancels each other. We only need to consider the electric field of the semicircle. Similarly, there are always two charge points that are symmetrical to the centre O, and thus the x-axis component of the electric field always got cancelled.



$$D = \frac{Q}{4\pi R^2} = \frac{\rho(\delta\theta)R}{4\pi R^2}\cos(\theta)$$

$$E = \frac{D}{\varepsilon_o} = \frac{\rho(\delta\theta)R}{4\pi R^2\varepsilon_o}\cos(\theta)$$

Therefore the electric field of the whole semicircle is:

$$E = \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{\rho(\delta\theta)R}{4\pi R^2\varepsilon_o}\cos(\theta) = -\frac{\rho}{2\pi R\varepsilon_o} = -\frac{5\ \mu C m^{-1}}{2\pi \times 5m \times 8.854 \times 10^{-12} F m^{-1}} = 18\text{kV}\ m^{-1}$$

The direction of the electric filed is shown below: