EGT0
ENGINEERING TRIPOS PART IA

Monday 12 June 2023 9.00 to 12.10

Paper 3

ELECTRICAL & INFORMATION ENGINEERING

*Answer **all** questions.*

*The **approximate** number of marks allocated to each part of a question is indicated in the right margin.*

Answers to questions in each section should be tied together and handed in separately.

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

Section A

1 **(short)** Using star-delta transformation, determine the current flowing in the resistor R_1 between nodes A and B. [10]

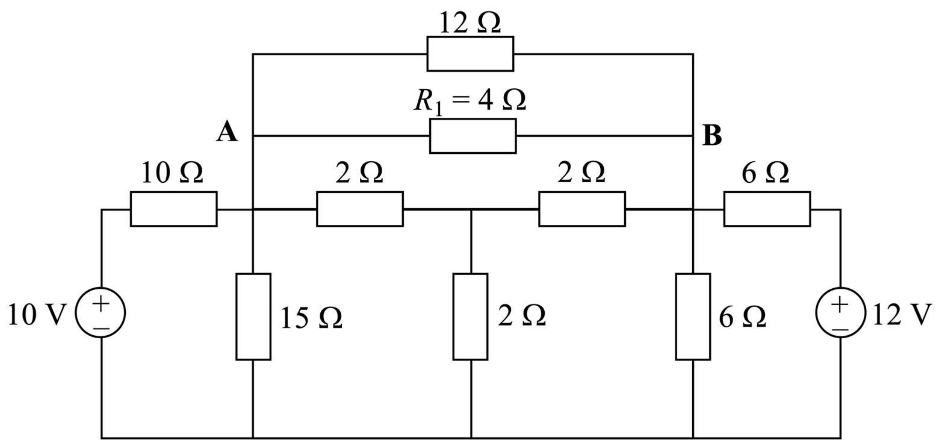

Fig. 1

2 **(short)** Calculate the total complex impedance of the circuit shown in Fig. 2. Find the magnitude and phase of the supply current with respect to the 230 V, 50 Hz voltage source.

[10]

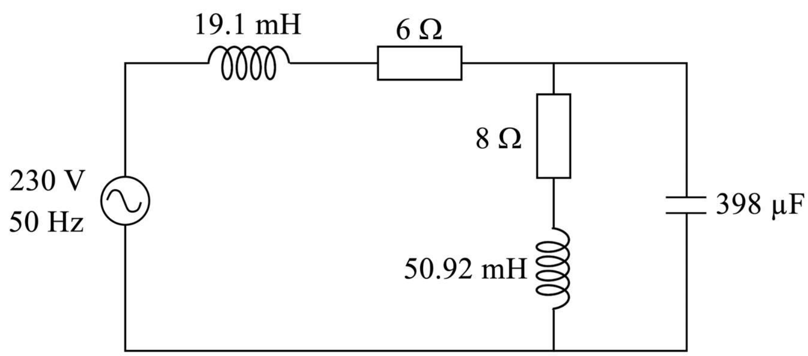

Fig. 2

(TURN OVER

3 **(long)** The amplifier with a depletion mode MOSFET in Fig. 3 is biased to achieve $V_{GS} = -3$ V, $V_{DS} = 8$ V and $I_D = 3$ mA. The gate resistor R_2 is 10 MΩ. The supply voltage V_{DD} is 20 V. The FET has small-signal parameters $g_m = 6$ mA/V and $r_d = 10$ kΩ. It can be assumed that the FET is ideal and that there is no gate current.

(a) Briefly explain how the FET is biased. [4]

(b) Find the values of R_1 and R_3 to set the desired operating point. [4]

(c) Draw the small-signal model of the circuit, assuming that the reactance of the capacitors are negligible. Hence derive the expressions for small-signal gain and output and input impedances. [10]

(d) The low frequency –3 dB point of the amplifier is dominated by C_{out} and is 20 Hz when a load resistor of 5 kΩ is connected to the output. Determine the value of C_{out}. You may assume that the reactance of C_S is small compared to R_3. [8]

(e) If C_{out} remains unchanged, what load resistor value is needed to maximise the signal power to the load? Determine the new low frequency –3 dB point with this load resistor. [4]

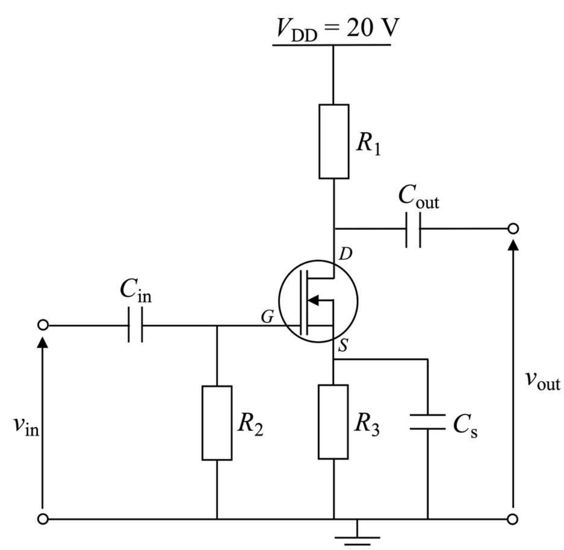

Fig. 3

4 **(short)** Derive the expression for the gain of the circuit shown in Fig 4. The operational amplifier is ideal. If R_1 = 1 kΩ, R_2 = 10 kΩ, C_2 = 20 pF, sketch the Bode magnitude plot of the circuit showing its key characteristics. You are not required to use graph paper. [10]

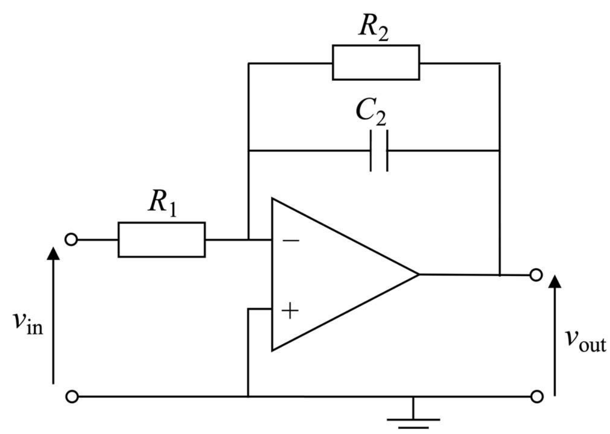

Fig. 4

5 **(long)** A large packaging machine consumes 200 kW of power when a 1 kV, 50 Hz supply is directly connected across it. The machine has a 0.85 lagging power factor. A feeder line with a complex impedance of $(0.8+j1.6)\ \Omega$ now supplies the machine from a 50 Hz voltage source.

(a) If the voltage at the machine terminals is 1 kV, calculate the feeder current, feeder power loss, and the source voltage. [12]

(b) Power factor correction is applied by connecting a capacitor in parallel with the machine. If 1 kV is maintained across the machine terminals, calculate the required value of this capacitor, the new feeder current, and the feeder power loss. [10]

(c) With the power factor correction capacitor still connected, if the source voltage is set at 1 kV, what will be the magnitude of the voltage across the machine terminals? [8]

SECTION B

6 **(short)**

(a) Explain what is meant by static 0 and static 1 hazards in combinational digital circuits. [2]

(b) A function F is defined as $F = \bar{A} \cdot \bar{C} + A \cdot D$. Determine the potential hazards and recommend solutions for these hazards. [8]

7 **(short)** A serial line carries digital data to a system with input X. The system is required to detect a sequence 010 and give an output Y at the end of the detected sequence. Only non-overlapping sequences should be detected (i.e., the output Y should only be high for the "0" underlined in the input sequence 1010101). J-K bistables are to be used in the design of the system.

(a) Draw the state diagram and state how many bistables are required. [4]

(b) Write down the state transition table for the system. [6]

8 **(short)**

(a) A certain memory chip has 11 address lines and 8 data lines. It is connected to a microprocessor with a 16-bit address bus and an 8-bit data bus. Determine the capacity of the memory chip in bytes. [2]

(b) Determine a Boolean expression for the $\overline{CS}$ input such that the memory chip appears in the microprocessor's memory map between locations $D800_H$ and $DFFF_H$. Draw a circuit showing how the memory chip should be connected to the microprocessor. [8]

9 **(long)** A 4-bit synchronous down counter starts from 15 (1111 in binary) and counts downwards to 0 (0000 in binary) and starts a new cycle again. It is to be designed using J-K bistables.

(a) Write down the complete truth table. [6]

(b) Construct the Karnaugh maps and derive the logic expressions for the J and K inputs. [6]

(c) Draw the complete circuit diagram. [12]

(d) Draw the signal at the bistable outputs during 10 clock cycles for a 1 GHz clock frequency. [6]

SECTION C

10 **(short)** Three metal plates A, B, and C are placed in parallel with air between them, and all have an area of 200 cm^2, as shown in Fig. 5. The distance between plates A and B is 2 mm, and the distance between plates B and C is 4 mm. Both plates A and C are connected to earth, but plate B has a total positive charge of $Q = 3.0\times10^{-7}$ C.

(a) What are the induced charges in plates A and C? [5]

(b) What is the potential V of plate B? [5]

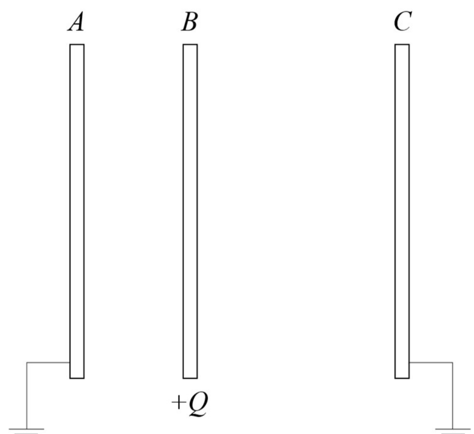

Fig. 5

11 **(short)** Three parallel infinitely long wires are placed in the same plane and adjacent wires are separated by a distance d. Each wire carries a current of I and all currents are flowing in the same direction, as shown in Fig. 6. The radius of the wire is significantly smaller than d. Find the positions at which the total magnetic flux density is zero. [10]

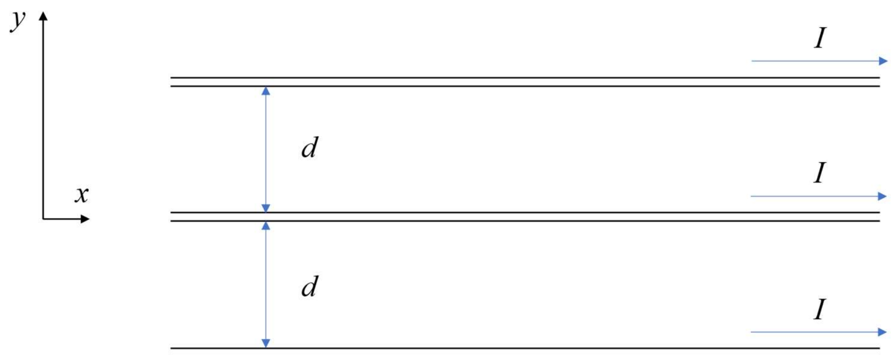

Fig. 6

12 **(long)** An air-filled hollow conducting sphere has outer and inner radii of $R_1 = 5.0$ cm and $R_2 = 4.0$ cm with its outer surface connected to earth, as shown in Fig. 7. A conducting concentric sphere with a radius of $R_3 = 2.0$ cm is placed inside the hollow sphere and it has a positive charge of $Q = 3.0\times10^{-8}$ C.

(a) What is the electric field at $R = 1.0$ cm, $R = 3.0$ cm and $R = 6.0$ cm? [15]

(b) What is the capacitance of the concentric spheres? [7]

(c) What is the electrostatic energy stored in the concentric spheres? [8]

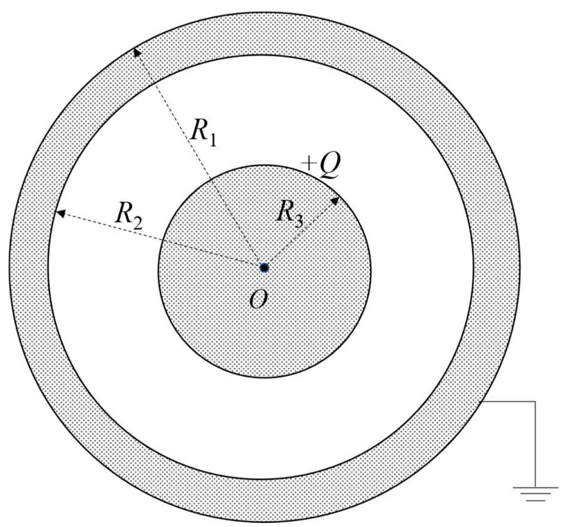

Fig. 7

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