Version OBA/2

EGT0
ENGINEERING TRIPOS PART IA

Monday 16 June 2025 9.00 to 12.10

Paper 3

ELECTRICAL & INFORMATION ENGINEERING

*Answer **all** questions.*

*The **approximate** number of marks allocated to each part of a question is indicated in the right margin.*

Answers to questions in each section should be tied together and handed in separately.

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM

CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

Section A

1 (**short**) Figure 1 shows an ac bridge circuit with an ac source of frequency ω. Find the frequency at balance in terms of R_3 and C. [10]

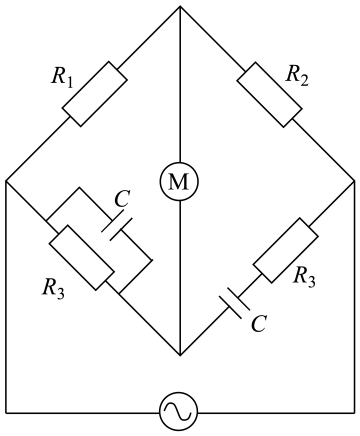

Fig. 1

2 (**short**) Calculate the current drawn from the 120 V rms supply if the supply frequency is 50 Hz in Fig. 2. What is the resonant frequency of this circuit? [10]

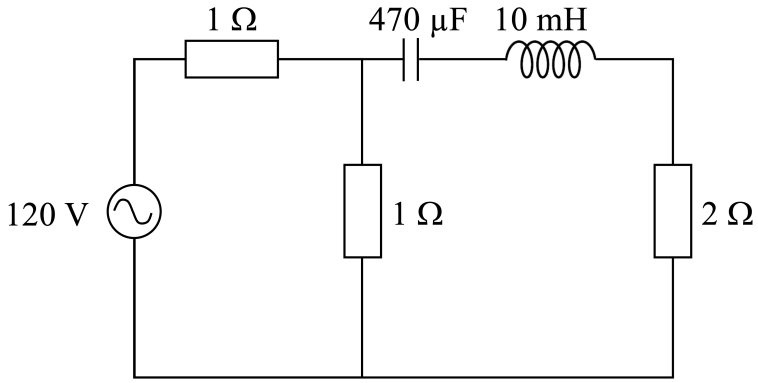

Fig. 2

3 (**short**) An op-amp circuit is connected with voltage source v_{in} through a co-axial cable in Fig. 3. The source has an output resistance R_s of 500 Ω. Determine the midband voltage gain v_{in}/v_{out} and the 3 dB frequency of the circuit. State any assumptions made. The op-amp is ideal. [10]

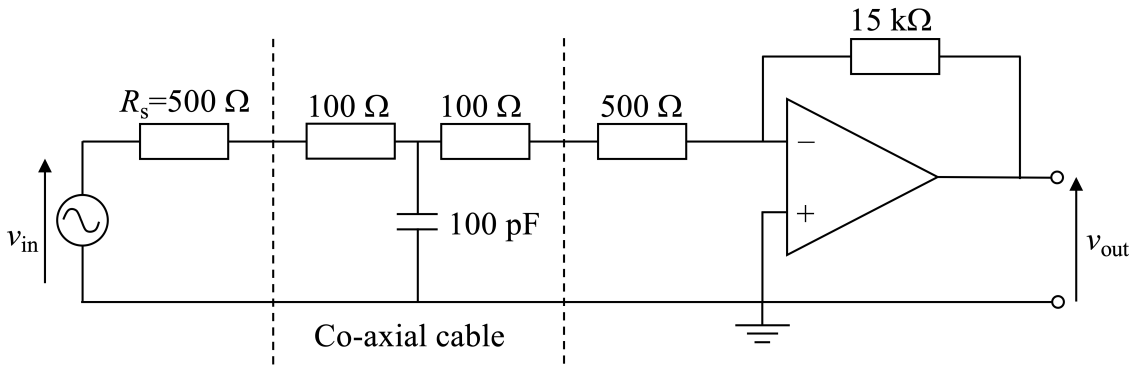

Fig. 3

4 (**long**) An FET is used in an amplifier circuit as shown in Fig. 4(a). The small signal parameters of the FET are g_m = 5 mS and r_D = 15 kΩ. The R_s = 6 kΩ and R_G=2 MΩ.

(a) Calculate the gain and the output impedance of the circuit. [12]

(b) Due to electrical interference, noise in the form of a voltage with 200 Hz frequency is induced in the drain of the FET. This noise can be represented by including a small voltage source v_N at the drain, as shown in Fig. 4(b). Draw the small signal equivalent circuit and by setting v_{in}=0, derive the expression for the contribution of this noise to the circuit's output voltage. [12]

(c) Determine the maximum amplitude of v_N if the noise contribution to the output must not exceed 30 μv. [6]

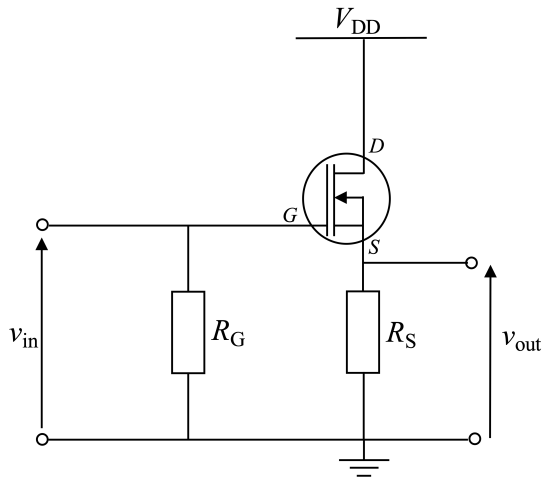

Figure 4 (a)

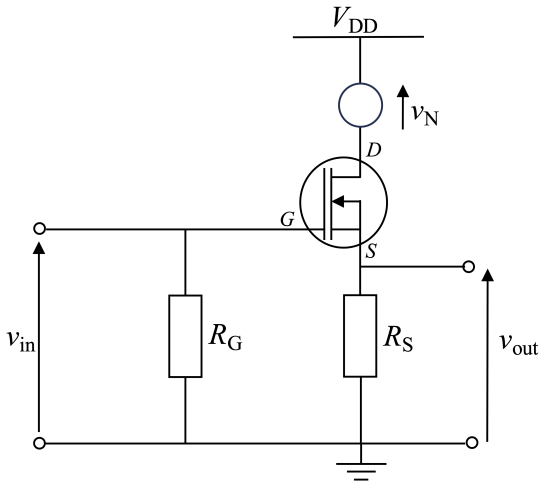

Figure 4 (b)

Fig. 4

5 (**long**) A crane lifts a mass of 4 kg at a speed of 1 ms^{-1}. The crane's 50 Hz AC motor can be modelled as a 50 mH inductance in series with a resistor R. The resistor dissipates a power equal to the output of the motor. State any assumptions made when answering the following questions:

(a) If the input current is 2 A when lifting this load, what is the power factor of the circuit? [8]

(b) If the crane is driven by an ac supply with a higher voltage through an ideal step-down transformer with a turns ratio of 20:1, what capacitance can be placed across the transformer's high voltage terminals to give the circuit a power factor of unity? [12]

(c) If instead of needing power factor correction, the transformer's winding losses for this load are known to be 3 W and 4 VARs, what will be the input high voltage and the power factor? [10]

Section B

6 (**short**) A half adder adds two single binary digits (A and B) and has two outputs, sum (S) and carry (C_{out}). A full adder circuit adds two binary digits but also accounts for a digit carried in (C_{in}) as well as out (C_{out}).

(a) Derive logical expressions for the outputs of the half adder in terms of its inputs and draw a circuit implementation using one XOR gate and other gates if needed. [4]

(b) Derive logical expressions for the outputs of the full adder in terms of its inputs and draw a circuit implementation using logic gates. [6]

7 (**short**) A two-bit counter implemented using D-type bistables is shown in Fig. X.

(a) Draw the state diagram for the two-bit counter. [5]

(b) What is the code implemented by this counter and why is this advantageous in certain applications? [2]

(c) How would you reconfigure the counter to reverse the sequence determined above? Draw the actual circuit implementation. [3]

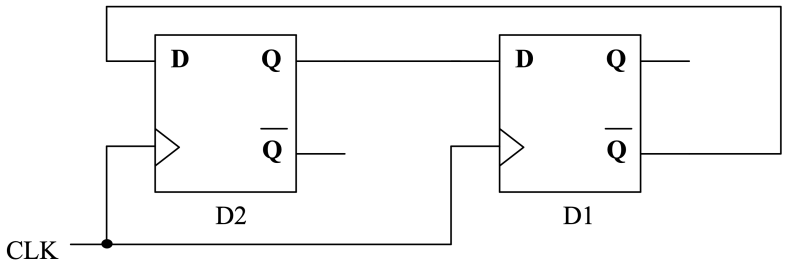

Fig. 5

8 (**short**) A 256 kilobyte memory chip has 16 data lines.

(a) How many address lines does the memory chip have? [4]

(b) In a microprocessor with 20 address lines, how many of these memory chips can be connected? What are the address ranges for the first and the third chips in hexadecimal format? [6]

9 (**long**)

(a) X and Y are two 2-bit unsigned binary numbers, where $Y > 1$. The 4-bit binary number P satisfies the equation:

$$P = (X)^2 + Y$$

Design a digital circuit that calculates the most significant bit and the least significant bit of P from the bits of X and Y. The circuit should be composed only of NOR gates and the smallest possible number of such gates should be used. [15]

(b) 2-bit binary unsigned numbers are received sequentially by a detector. Each of these numbers is greater than 1. The output Z of the detector becomes 1 if the current value of the number received is greater than 2 and the value of the previous number received was equal to 2. The output Z is otherwise 0.

(i) Draw a state diagram for the system. [6]

(ii) State how many JK bistables will be needed to implement the detector and draw a state transition table (assume that unused states are never reached). [5]

(iii) Derive simplified Boolean expressions for the J inputs of the bistables. [4]

Section C

10 (**short**) Assume that charge of Q is uniformly distributed on a sphere of radius R.

(a) Derive expressions for the electric field inside and outside the sphere. [4]

(b) Derive an expression for the capacitance of the sphere (the potential at infinity is zero). [4]

(c) With $\varepsilon_0 = 8.85410^{-12}$ F m^{-1}, estimate the radius of the sphere if the capacitance is 1 pF. [2]

Write down each step and state clearly any approximations made.

11 (**short**) Two coaxial cylindrical surfaces have radii r_1 and r_2, $r_2 > r_1$, height h, and $h \gg r_2$. The inner cylindrical surface carries a charge of $+Q$, the outer cylindrical surface carries a charge of $-Q$, and the two cylindrical surfaces rotate along the central axis at a uniform angular velocity ω, as shown in Fig. 6. Ignore fringe effects.

(a) Derive expressions for the current densities on the two cylindrical surfaces. [5]

(b) Derive expressions for the distribution of magnetic flux density $\boldsymbol{B}$ in the regions inside the central cylinder, between the two cylinders, and outside the outer cylinder. [5]

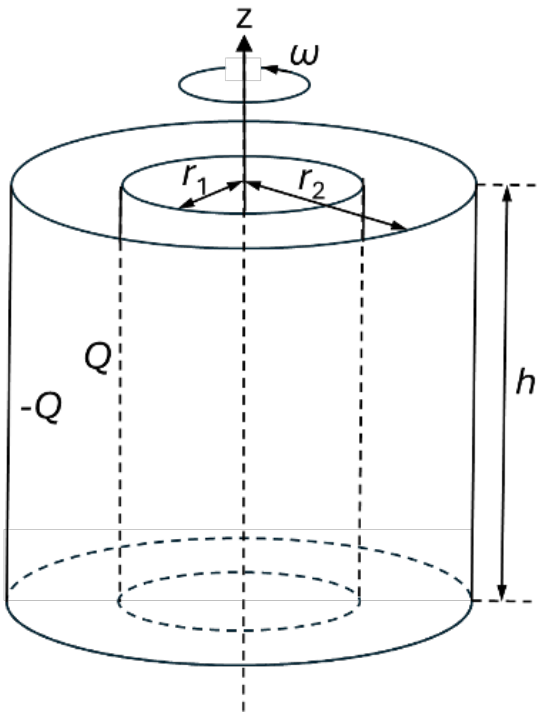

Fig. 6

12 (**long**) The area of the two plates of a parallel plate capacitor is A, and the distance between them is d. There is a parallel dielectric plate of the same area with a thickness of t and a dielectric constant of ε_r between them, as shown in Fig. 7. Initially, switch S is ON, which charges the capacitor to a voltage of V. Treat the problem as capacitors in series and ignore the fringe effect.

(a) Calculate the capacitance of the capacitor with the dielectric plate. [6]

(b) Disconnect the power supply by switching off the switch S and pull out the dielectric plate. How much work needs to be done? [12]

(c) If the dielectric plate is pulled out without disconnecting the power supply, how much work will be done? [12]

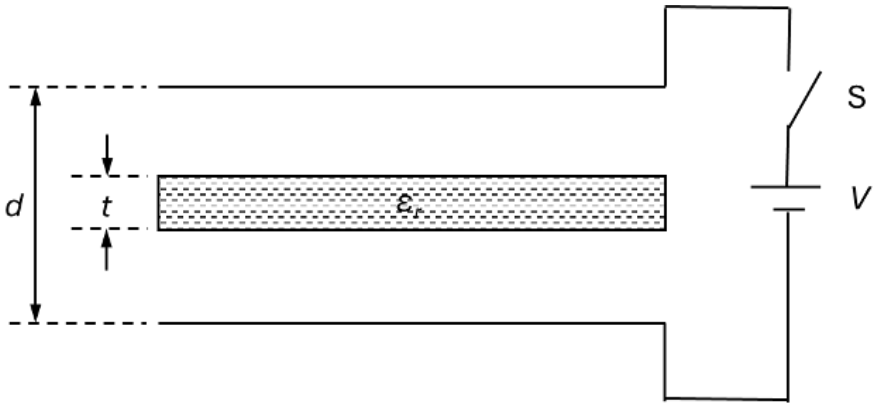

Fig. 7

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