Version QC/8

EGT0
ENGINEERING TRIPOS PART IA

Monday 13 June 2022 9.00am to 12.10pm

Paper 3

ELECTRICAL & INFORMATION ENGINEERING

*Answer **all** questions.*

*The **approximate** number of marks allocated to each part of a question is indicated in the right margin.*

Answers to questions in each section should be tied together and handed in separately.

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

Section A

1 (short)

(a) Derive the Norton equivalent circuit of the circuit shown in Fig. 1 across terminals AB. [4]

(b) For the case R = 10 Ω and I_0 = 3 A, derive the corresponding Thévenin equivalent circuit. [3]

(c) Consider the case where the current source has an internal resistance of 10 kΩ. Determine the power dissipated in the entire system. [3]

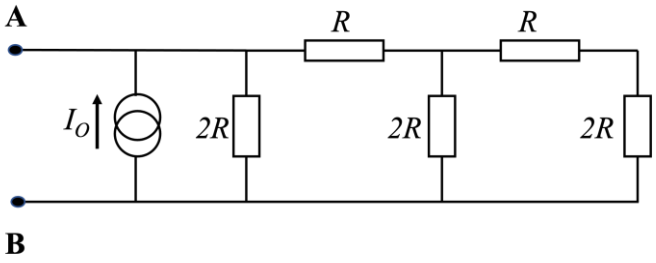

Fig. 1

2 (short) A general voltage amplifier is shown in Fig. 2.

(a) For the case where the output is an open-circuit, determine the voltage gain. [1]

(b) A load resistor, R, is connected across the output terminals BC. Determine the new voltage gain of the resulting circuit. [3]

(c) For the case that the source of v_{in} has zero internal resistance and the value of $R = R_{out}$, determine the power gain of the circuit. [4]

(d) Show that the condition for maximum transfer of power to the load is that $R = R_{out}$. [2]

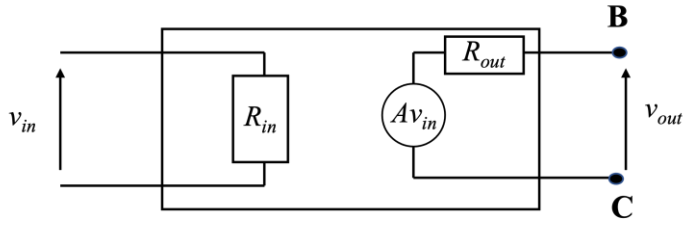

Fig. 2

3 (long) The input characteristic of an n-channel enhancement-mode field effect transistor is shown in Fig. 3a. The supply voltage, V_{DD} is 10 V and R_1 = 4.25 MΩ.

(a) The transistor is to be used at an operating point set as V_{DS} = 5 V, V_{GS} = 1.5 V and I_D = 4 mA, in a common-source configuration as shown in Fig. 3b. Determine the values of the resistors R_2 and R_3 required to achieve the desired operating point, stating any assumptions made. [4]

(b) At this operating point, the small-signal drain resistance r_d = 10 kΩ. From the graph in Fig. 3a, determine the small-signal mutual conductance, g_m. [6]

(c) Draw the small-signal equivalent circuit of the amplifier with the salient features clearly labelled. [3]

(d) Calculate the input resistance, output resistance and voltage gain of this circuit. [12]

(e) A voltage of amplitude 400 mV from a signal source with internal resistance 100 Ω is connected to the input terminals of the amplifier. Calculate the resulting output voltage. [5]

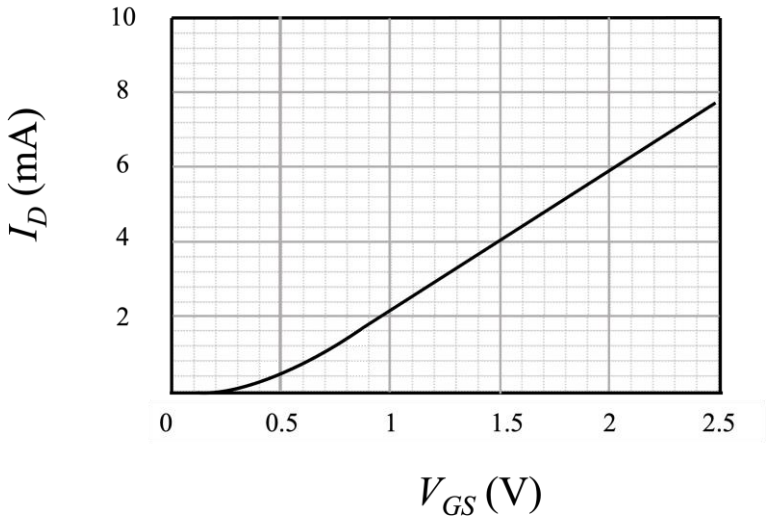

Fig. 3 (a)

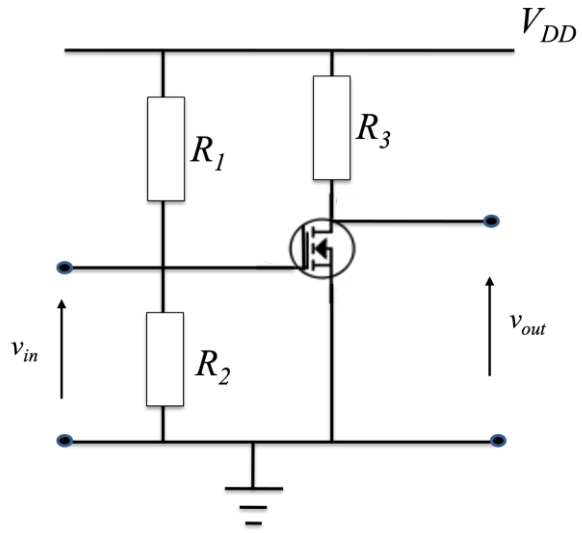

Fig. 3 (b)

4 (short) The equivalent circuit for a 50 Hz power transformer is shown in Fig. 4.

Under open-circuit conditions, $\tilde{V}_{out}$ is measured to be 66 kV $\angle 0$ with $\tilde{V}_{in} = 11$ kV $\angle 0$. The corresponding input current is measured to be $\tilde{I}_{in} = 0.1$ A at a power factor of 0.8 lagging.

Under short-circuit conditions, $\tilde{V}_{in}$ is measured to be 0.5 kV $\angle 0$ with an input current of 3A and an input power of 270 W.

(a) What is the turns ratio of the transformer? [2]

(b) Determine the hysteresis and eddy current losses (i.e., those in R_0) in the transformer when it is connected to an open circuit. [3]

(c) Determine the values of the leakage reactance and magnetising reactance of the transformer. In an ideal transformer, what would these values be? [5]

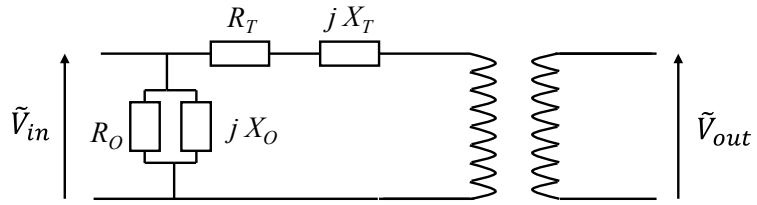

Fig. 4

5 (long) A non-inverting Operational amplifier circuit is shown in Fig. 5a.

(a) Derive an expression for the voltage gain of the circuit, stating any assumptions made. [6]

(b) Two capacitors, C_1 and C_2 are now added as shown in Fig. 5b, where $C_1 >> C_2$. Derive an expression for the voltage gain of this circuit as a function of frequency and sketch what its magnitude looks like, clearly labelling the salient features. [12]

(c) The circuit in Fig. 5b is required to have a mid-band voltage gain of 100 and upper and lower -3 dB frequencies of approximately 1 MHz and 100 Hz, respectively. Determine appropriate values for R_2, C_1 and C_2 assuming that R_1 = 5 kΩ. State any approximations made. [10]

(d) For the case where R_2 is replaced with an inductor, briefly describe how you expect the gain to vary as a function of frequency. [2]

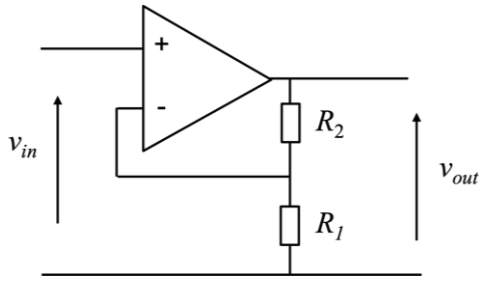

Fig. 5a

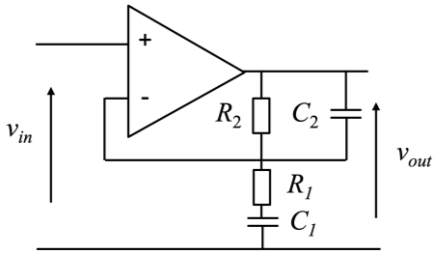

Fig. 5b

SECTION B

6 (short)

(a) Several 64k bit memory devices, each with four data lines, are to be connected to a microprocessor with an 8-bit data bus.

(i) How many and what kinds of connections will there be on each memory device? [3]

(ii) How many devices are needed to make 64k bytes of memory? [1]

(b) (i) What is a shift register? [3]

(ii) The outputs from the final two stages of a 4-stage shift register are fed back to the input to the first stage via an exclusive-OR gate. How many steps are there in the longest sequence of the shift register states? [3]

7 (short) Before the following PIC12F629 code is executed, the contents of memory locations 0x30 and 0x31 are the decimal numbers 20 and 50 respectively:

```
        movlw 0x31;
        movwf FSR;
        call sr;
        decf FSR;
        call sr;
        sleep;
.....

sr      rrf INDF;
        movlw 0x10;
        addwf INDF;
        return;
```

(a) Explain the function of each step; [5]

(b) What are the contents of W and memory locations 0x30 and 0x31 after the code has executed? [3]

(c) Determine the number of clock cycles and time taken to execute the code assuming a 20 MHz clock. [2]

8 (short) The circuit in Fig. 6 shows a simple form of a 4-bit digital-to-analogue converter. Digital "1" is assumed to be 5 V and digital "0" is assumed to be 0 V.

(a) Briefly explain the principle of operation. Which of these inputs represent the least significant bit and most significant bit, respectively? [5]

(b) If the value of R is 1 kΩ and the operational amplifier is considered to be ideal, determine the input resistance at the terminals S_1 and S_2. [2]

(c) Determine the output voltage V_0 if the digital signal 1011 is present at the inputs S_3 S_2 S_1 S_0. [3]

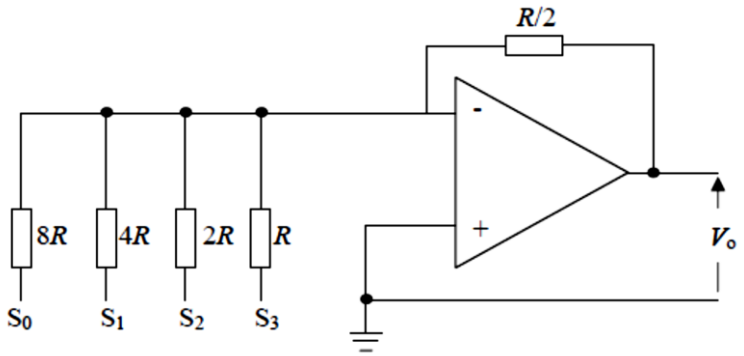

Fig. 6

9 (long)

(a) Explain the main differences between combinational and sequential logic. [4]

(b) Logic values A, B, C and D represent the four bits of a binary number in the range of 0 to 15. A combinational logic circuit is to be devised which outputs 1 if the number is greater than 5 and less than 15; it is to output 0 otherwise. See Fig. 7 for details of the significance of the bits.

(i) Construct a truth table and map the corresponding expression. [4]

(ii) Show how to implement efficient logic systems to realise this function in terms of an expression, using minimum numbers of:

NAND gates; [8]

NOR gates. [8]

(c) Explain how the Karnaugh map may be used to assist in identifying static hazards that might be present in your designs, and show how these may be corrected. [3]

(d) It is often stated that the use of the Karnaugh map technique for simplifying logic functions leads to a solution requiring the minimum number of logic gates. Comment briefly on this proposition. [3]

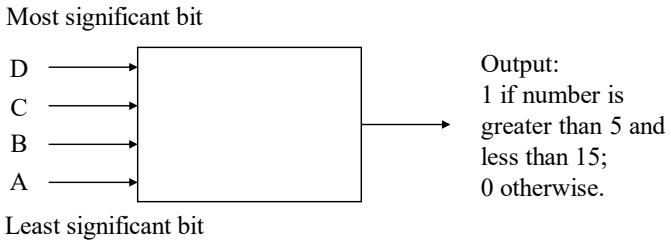

Fig. 7

SECTION C

10 (short) A coaxial cable consists of an inner conductor and an outer conductor with radii of R_1 = 0.8 mm and R_2 = 1 mm, respectively, shown in Fig. 8. The inner conductor is a hollow cylinder of length L = 2 m. The gap in between is filled with a dielectric material of relative permittivity ε_r = 1000. The inner conductor is biased at V = 5 V, while the outer conductor is connected to earth.

(a) Calculate the charge on the inner conductor. [6]

(b) What is the capacitance of the coaxial cable? [4]

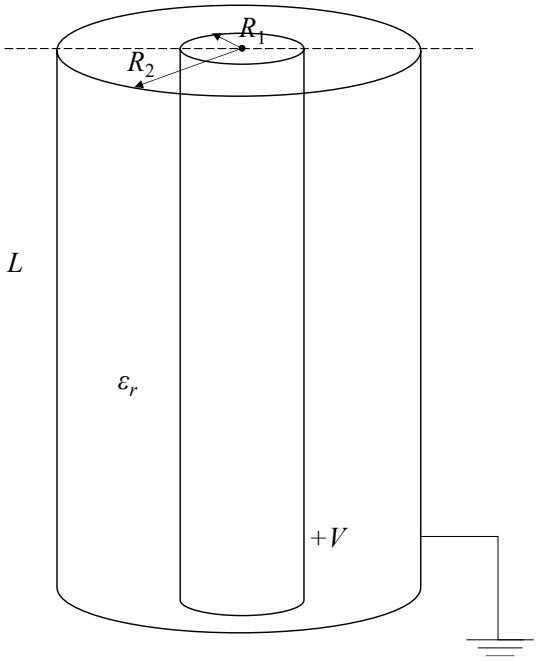

Fig. 8

11 (short) Two straight infinitely long wires are placed in the same plane and are parallel to each other as shown in Fig. 9. The distance between the two wires is L = 40 cm. The two wires each carry a current $I = I_1 = I_2$ = 20 A but with opposite directions of flow.

(a) What is the direction and magnitude of the magnetic flux density at a point midway between the two parallel wires (in the same plane)? [4]

(b) What is the magnetic flux passing through a rectangle in the plane of the two wires that is placed in the middle with $L_1 = L_2$ = 10 cm, and d = 25 cm? [6]

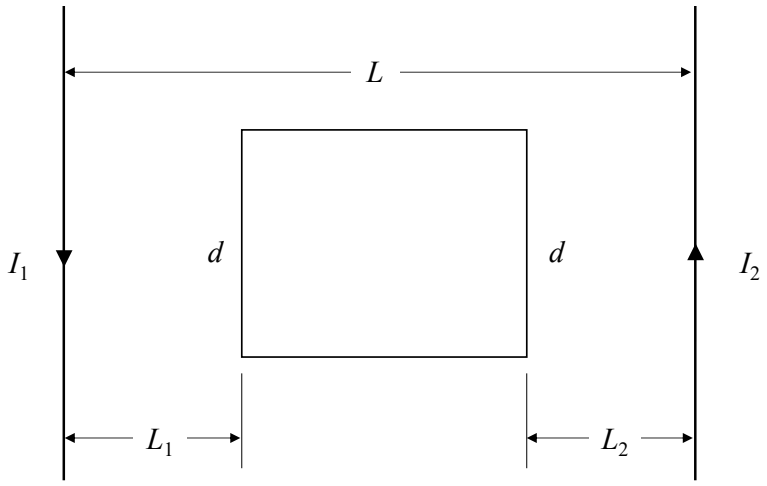

Fig. 9

12 (long)

(a) What is the magnitude and direction of the electric field at a position 5 m from a single point charge Q in air? [5]

(b) What is the magnitude and direction of the electric field at a position (O) that has 5 point charges of Q arranged at angles θ = 0°, +/-60° and +/-90° with R = 5 m in air as shown in Fig. 10a? [10]

(c) A line of charges with positive charge density ρ = 5 μC m^{-1} is placed in air. It has a shape as shown by Fig. 10b, where the semicircle has a radius of R = 5 m and the two straight sections each have a length of L = 5 m. What is the magnitude and direction of the total electric field at the centre of the semicircle (O)? [15]

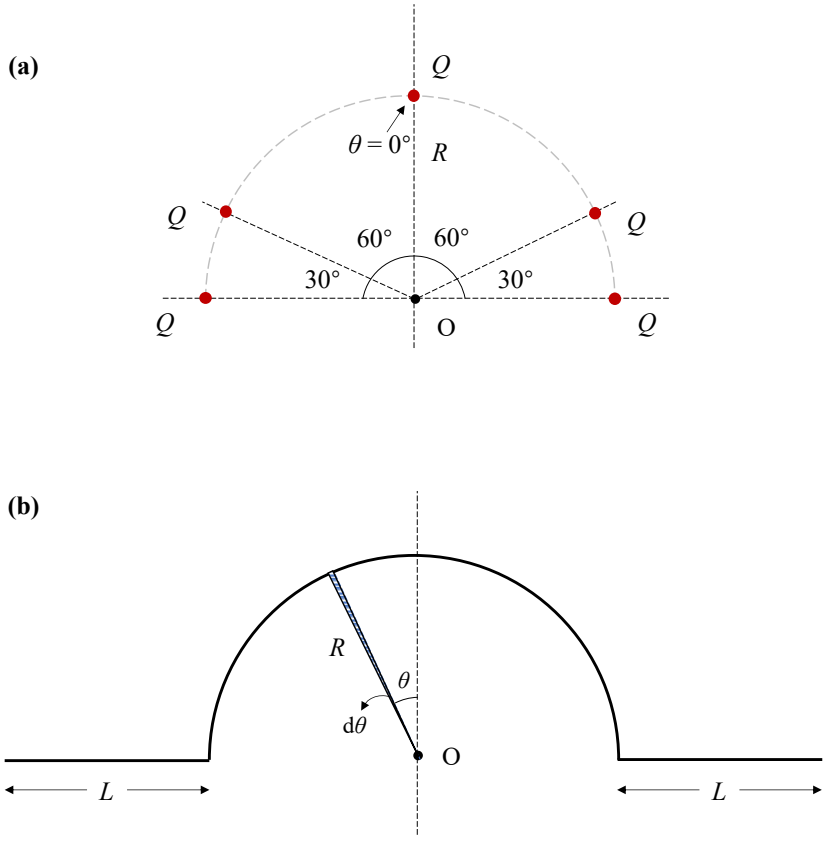

Fig. 10

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