Version MJC/4

EGT2
ENGINEERING TRIPOS PART IIA

Tuesday 23 April 2024 14:00 to 15:40

Module 3B1

RADIO FREQUENCY ELECTRONICS

Answer not more than ***three*** *questions.*

All questions carry the same number of marks.

The ***approximate*** *percentage of marks allocated to each part of a question is indicated in the right margin.*

Write your candidate number ***not*** *your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Supplementary page: Smith Chart (Question 1)
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 (a) The output of an RF oscillator has an impedance of 25 – j20 Ω at a frequency of 220 MHz. Design an impedance matching circuit, using a pair of components with the Q-method, to match the output to 75 Ω. [20%]

(b) Draw a schematic block diagram of a Vector Network Analyser (VNA) and briefly describe how it operates to measure the S-parameters for a 2-port network, particularly explaining why calibration is important. [20%]

(c) The S11 parameter at the input of an RF amplifier has been measured to be $0.86 \angle 52°$ when operating in a 50 Ω system at a frequency of 915 MHz.

(i) Plot S11 on the Smith chart and read off the complex impedance values at this point. What series passive components do these correspond to? [15%]

(ii) Design an impedance matching circuit using a length of transmission line and a series capacitor to match the input to 50 Ω. If the transmission line comprises a length of coaxial cable with a capacitance of 85 pF m^{-1}, what physical length is required in the matching circuit? [25%]

(iii) With the aid of the Smith chart, design an alternative impedance matching circuit comprising a pair of passive components to match the amplifier to 50 Ω at the operating frequency. [20%]

A Smith chart is attached to the back of the question paper. It should be detached and handed in with your answers.

2 (a) A phase locked loop (PLL) used to recover a square wave clock signal waveform from a digital bit stream is shown in Figure 1.

(i) Briefly describe the function of each component in the operation of the loop and explain the input/output functions of labels X, Y and Z. [10%]

(ii) If the XOR gate uses 5V logic and the VCO has a response of 2 MHz V^{-1}, derive an expression for the transfer function of the loop and hence find the RC time constant required for the loop to have a transient step response overshoot of 10%. [50%]

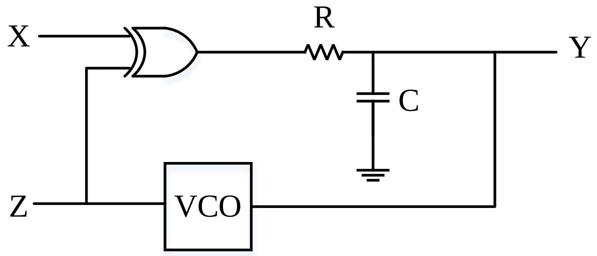

Fig. 1

(b) A circularly polarised antenna is made using a pair of cross polarised antennas each with an input impedance of 50 Ω fed by microstrip transmission lines and a Wilkinson splitter. The transmission lines are made on 0.8 mm thick circuit board with $\epsilon_r = 4$.

(i) What track width should be used to create a characteristic impedance of 50 Ω? [20%]

(ii) What should the difference in the feeding track lengths of the antennas be if the operating frequency is 3 GHz? [20%]

3 (a) Draw the schematic circuit diagram of a 2-pole *Voltage Controlled Voltage Source* (VCVS) low-pass filter and show how the circuit can produce a Butterworth filter response with the following transfer function:

$$\left|\frac{V_o}{V_i}\right| = A\left[1 + \left(\frac{f}{f_c}\right)^4\right]^{-\frac{1}{2}}$$

where V_O and V_i are the output and input voltages respectively, and f_C is the –3 dB cut-off frequency. How should the circuit be modified to give a high-pass response instead? [35%]

(b) Design a 4-pole VCVS band-pass IF filter for a Superhet receiver circuit, with steep cut-offs either side of the 1 MHz ± 200 kHz pass-band. Using 1 kΩ resistors where appropriate, give the values of other passive components used. Justify your choice of filter type. A 4-pole VCVS filter design table is given on the facing page in Table 1. [25%]

(c) A Colpitts oscillator is to be designed to produce an output signal of 1090 MHz across a load impedance of 300 Ω. The output should have high spectral purity and have a power around 10 dBm. The supply voltage is +6 V d.c.

(i) Draw a schematic circuit diagram for a Colpitts oscillator circuit and briefly describe the function of each of the components shown. [10%]

(ii) Select values for the passive components, using an inductor value of 5 nH with a Q-factor of 20. [10%]

(iii) What is the effect of the transistor input capacitances on the oscillation frequency when the transistor has the following parameter values: f_t = 8 GHz, c_{cb} = 0.25 pF and h_{fe} = 200? How could this effect be compensated by the addition of some further circuit components to enable electrical tuning? [20%]

(cont.

Table 1. 4-pole VCVS filter design table

Bessel		Butterworth		Chebyshev (0.5 dB)	
f_n	A	f_n	A	f_n	A
1.432	1.084	1.000	1.152	0.597	1.582
1.606	1.759	1.000	2.235	1.031	2.660

(TURN OVER

4 An aircraft radar receiver uses a two-stage RF amplifier to boost the signal from an antenna by 35 dB when weak signals are being detected. The system is based on a 75 Ω characteristic impedance and operates at 1030 MHz, with matched input and output impedances, and operates with a supply voltage of +9 V d.c. The amplifier circuit includes a parallel resonant LC circuit, connected between the mid-stage coupling node and ground, to define the amplifier response pass-band.

(a) Draw a schematic circuit diagram of a suitable two-stage transistor amplifier and briefly describe the function of each of the components used. [20%]

(b) Calculate the values of the passive components in the amplifier circuit to achieve the net gain required. You may assume that suitable high-frequency transistors are available and that the inductor, L, has a value of 1.2 nH. [25%]

(c) Briefly describe the *Miller Effect* and how it can limit the bandwidth of RF amplifier circuits. What steps can be taken to mitigate these effects? [15%]

(d) In order to minimise costs, some low cost transistors with the following properties have been identified as potential candidates for use in this application:

h_{fe} = 150, f_t = 15 GHz, c_{cb} = 0.25 pF, c_{oe} = 0.20 pF

Estimate the upper −3 dB roll-off frequency for one stage of the loaded amplifier circuit and hence comment if these transistors are suitable for this application. [25%]

(e) If the resonant LC circuit inductor has a series resistance of 0.2 Ω at the frequency of operation, calculate the resulting bandwidth of the amplifier, ignoring any frequency limitations introduced by the transistors. [15%]

END OF PAPER

Answers:

1) (a) C = 47pF, L = 38.3nH
   (c) (i) 20Ω 17.4nH
   (ii) 1pF, 7.7mm
   (iii) 0.63pF in parallel, 1.16pF in series.
2) (a) (ii) 34ns
   (b) (i) 1.4mm
   (ii) 1.25cm
3) (b) $582\Omega\,, 222pF$ 1.66kΩ, 129pF   582Ω, 119pF   1.66kΩ, 205pF
   (c) C=8.52pF, R3 = 100Ω R1=1kΩ R2=670Ω Rd=27Ω
4) (b)   Cf=19.9pF, R4= 75Ω, R3 = 5Ω, R1 = 100Ω R2=800Ω C=1nF
   (d) 1GHz
   (e) 233MHz

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ENGINEERING TRIPOS PART IIA

XXday YY April 2024, Module 3B1, Question 1

Candidate No.

Smith Chart for Question 1 – to be detached and handed in with script.