Version OBA/2

EGT1
ENGINEERING TRIPOS PART IIA

Tuesday 03 May 2022 9:30 to 11:10

Module 3B2

ELECTRICAL ENGINEERING

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper.

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM

CUED approved calculator allowed.

Engineering Data Book.

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 (a) Explain how field-programmable gate arrays (FPGA) implement logic functions, such as gates, in a programmable way. How are the inputs and outputs of a logic function realised in this concept? In what way does this differ from complex programmable logic devices (CPLD)? Which circuit elements can implement the programmable part representing logic functions in an FPGA? [30%]

(b) Which two ways of describing the behaviour of a logic block (entity) exist in VHDL? What is the key difference between both? [20%]

(c) Which function is represented by the VHDL code in Fig. 1? Simplify the function and write it as a product of sums or a sum of products. [30%]

(d) Derive a function in standard binary coded decimal (BCD) that outputs TRUE (1) for every prime number up to 15 as sum of products (0 and 1 are not considered prime numbers). In the application, the previous and subsequent processing steps do not evaluate multiples of 5 so that these can return any result. Simplify this function to use as few terms as possible. [20%]

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY Q1 IS
      PORT ( x :  IN STD_LOGIC_VECTOR(4 DOWNTO 1);
             f :  OUT STD_LOGIC );
END Q1;

ARCHITECTURE Behavior OF Q1 IS
      SIGNAL mysig1 :  STD_LOGIC_VECTOR(4 DOWNTO 1) := "0000";
      SIGNAL mysig2 :  STD_LOGIC_VECTOR(4 DOWNTO 1) := "0000";
      CONSTANT one :  STD_LOGIC_VECTOR(4 DOWNTO 1) := "1111";
BEGIN
     mysig2 <= (x(1) AND NOT x(2) AND x(3)) OR (x(1) AND x(4)
AND x(2) AND NOT x(3));
      WITH x SELECT
           f <= '0' WHEN one,
                '0' WHEN mysig1,
                '0' WHEN "1001",
                '0' WHEN mysig2,
                '1' WHEN OTHERS;
     mysig1 <= (x(1) AND NOT x(4)) OR (x(1) AND x(3)) OR (x(1)
AND x(2) AND NOT x(1) AND x(4));
END Behavior;
```

Fig. 1

2 Consider the circuit shown in Fig. 2.

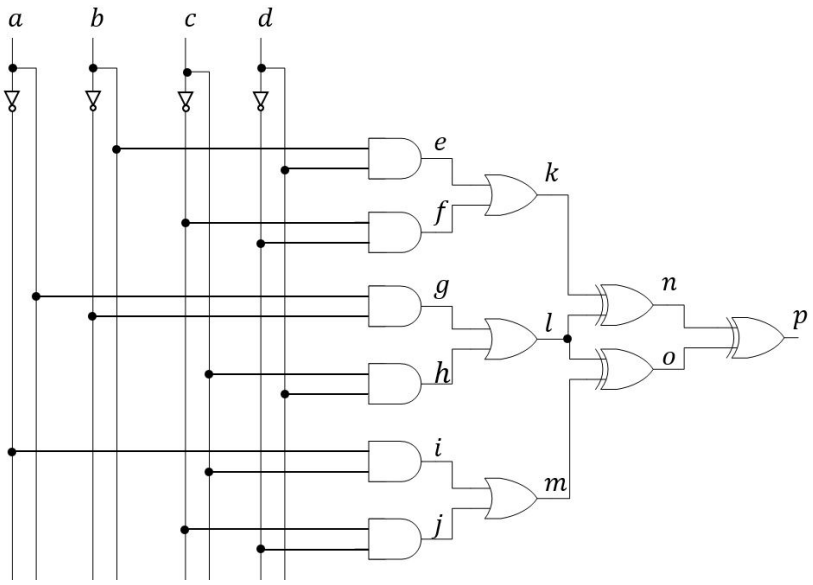


Fig. 2

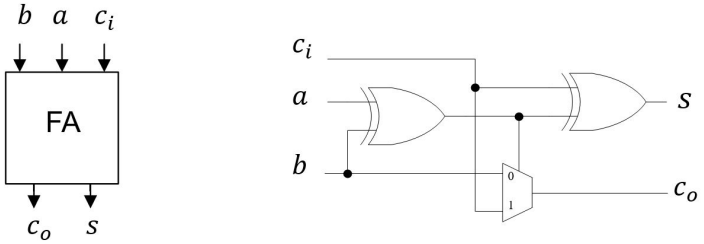


Fig. 3

(a) Find the simplest expression for the output p, where $p = f(k, l, m)$. [20%]

(b) To implement the circuit in Fig. 2 with minimum number of lookup table(s), how many inputs do each of the lookup table(s) require? Explain your answer. [20%]

(c) If only 3-input lookup tables (3-LUTs) are available, what is the minimum number of 3-LUTs required to implement this circuit? Indicate the input and output of each LUT according to the node names in Fig. 2. Mark unused input(s) of a lookup table with X. Do not attempt to simplify the gate-level circuit shown in Fig. 2. [40%]

(d) Using the Full-adder (FA) shown in Fig. 3, implement a logic circuit to subtract two 4-bit numbers. [20%]

3 (a) Give two disadvantages of the use of resistive load compared to transistor (active) load in MOS logic circuit implementations. [10%]

(b) The propagation delay and power dissipation values of different technologies are given in Fig. 4.

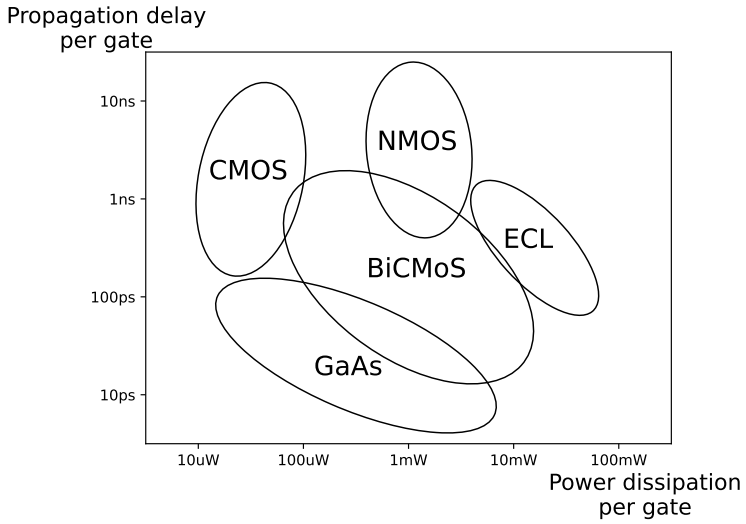


Fig. 4

(i) Suggest a technology for an integrated digital electronics device with a long-lasting battery, operating around 1-2 GHz. Give your reasoning. [10%]

(ii) Compare NMOS and CMOS from the perspectives of power consumption, manufacturing cost and area efficiency. [20%]

(c) A CMOS 2-input NAND gate is given in Fig. 5. Take $k'_N = 2k'_P$. Use

$$k' = \frac{\mu\varepsilon_{ox}}{t_{ox}},$$

$$k = k'\left(\frac{W}{L}\right),$$

where k is the transconductance parameter, μ is the carrier mobility, ε_{ox} is the permittivity of the oxide layer, t_{ox} is the oxide thickness and $\left(\frac{W}{L}\right)$ is the width/length ratio of the device. For NMOS transistors, take $\left(\frac{W}{L}\right) = 5$.

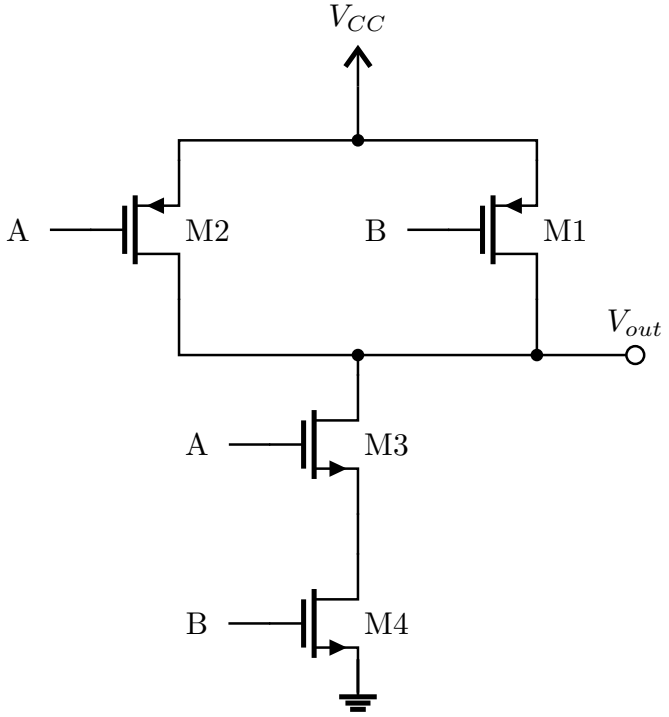


Fig. 5

(cont.

(i) Find the required $\left(\frac{W}{L}\right)$ ratio for PMOS transistors of the NAND gate in Fig. 5 such that the rise time, t_r^{NAND}, for the output when the input is AB=00, is equal to the fall time, t_f^{NAND}. [15%]

(ii) Due to a fabrication error, $\left(\frac{W}{L}\right)$ for M2 is 20% less than what it should have been when matched properly. How do you think this will impact the overall operation of the gate? [15%]

(iii) Draw a transistor-level implementation of a CMOS 2-input NOR gate. [15%]

(iv) Find the required $\left(\frac{W}{L}\right)$ ratio for all transistors of the CMOS 2-input NOR gate, if the fall time of NOR gate, t_f^{NOR}, when NOR input is AB=11, is equal to the fall time of NAND gate, t_f^{NAND}, and the rise time of NOR gate, t_r^{NOR}, is equal to the rise time of NAND gate, t_r^{NAND}, when NAND input is AB=00. [10%]

(v) Both NAND and NOR gates are universal, i.e., any logic function can be expressed solely by NAND or NOR gates. Which one, i.e., NAND or NOR, is a better choice in terms of area efficiency? Give your reasoning. [5%]

4 (a) What are the advantages and disadvantages of Schottky barrier diodes for logic gates compared to PN diodes? [10%]

(b) How is the switching frequency of a bipolar transistor impacted by charge storage? How can this be mitigated? [20%]

(c) Consider the circuit shown in Fig. 6. Two inputs, A and B are provided for an output V_{out}.

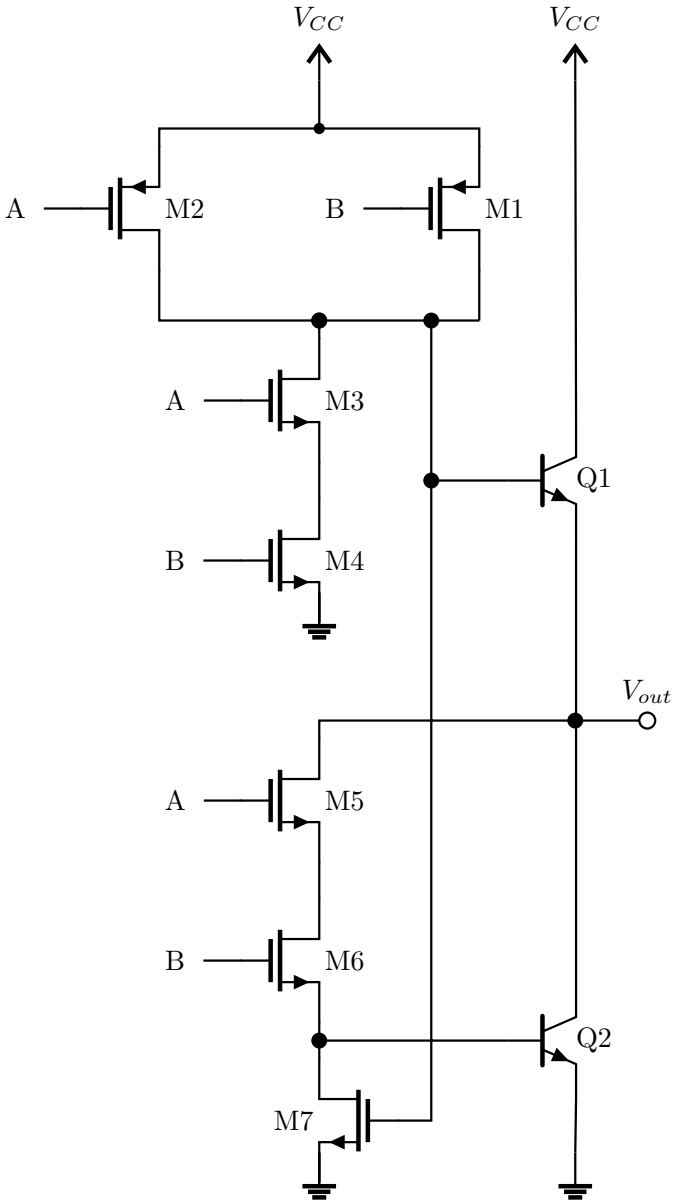
(i) Which technology is used for this circuit? [10%]

(ii) Which logic function is implemented by this circuit? [10%]

(iii) Explain the operation of this circuit for AB=[00,10,11]. Comment on which transistors are ON and which are OFF. [30%]

(iv) The active loads M3, M4 and M7 are all NMOS. Briefly explain why active loads are NMOS rather than PMOS. [10%]

(v) Briefly explain why the amplifier transistors, Q1 and Q2, are both NPN, rather than PNP. [10%]



NAND.pdf

Fig. 6

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Short Answers

1 (c) $\overline{x}_1$

2 (a) $k \oplus m$ (b) 4

3 (c)(i)2.5 (c)(iv) 1.25 (NMOS), 10 (PMOS)