Version OBA/2

EGT2
ENGINEERING TRIPOS PART IIA

Tuesday 09 May 2023 14.00 to 15.40

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS

Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM

CUED approved calculator allowed

Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 (a) Briefly discuss the advantages and disadvantages of implementing logic functions with multiplexers, ROMs, LUTs, and PLAs. [20%]

(b) Consider the VHDL code in Fig. 1. Derive the logic function and draw a circuit implementing this function. [30%]

(c) A synchronous 3-bit up/down counter with a Gray code sequence is needed. The counter should use J-K flip-flops and should count up when the UP/DOWN control input is 1 and count down when the control input is 0.

(i) Design the counter by drawing the state diagram and the state table. [20%]

(ii) Determine the Boolean functions for the J-K flip-flop inputs and draw a circuit implementation. [30%]

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY Q1 IS
      PORT ( x :  IN STD_LOGIC_VECTOR(1 TO 3);
             f :  OUT STD_LOGIC );
END Q1;
ARCHITECTURE Behavior OF Q1 IS BEGIN
      WITH x SELECT
           f <= '0' WHEN "001",
                '0' WHEN "011",
                '0' WHEN "101",
                '0' WHEN "111",
                '1' WHEN OTHERS;
END Behavior;
```

Fig. 1

2 (a) Explain the differences between Mealy and Moore sequential circuits. [10%]

(b) Figure 2 shows the implementation of a sequential circuit. Is this a Mealy or a Moore configuration? Explain your answer. [20%]

(c) The circuit of a 2-bit comparator is shown in Fig. 3. It compares two binary numbers, *A* and *B*, each of which are two bits, and produces their relation such that one number is less than, or equal to, or greater than the other.

(i) Build the truth table and find the output functions. [30%]

(ii) Implement the output functions using either a ROM or a PLA. Comment on your choice. [20%]

(d) Using only 2-bit comparator circuits, as shown in Fig. 3, implement a 4-bit comparator circuit. [20%]

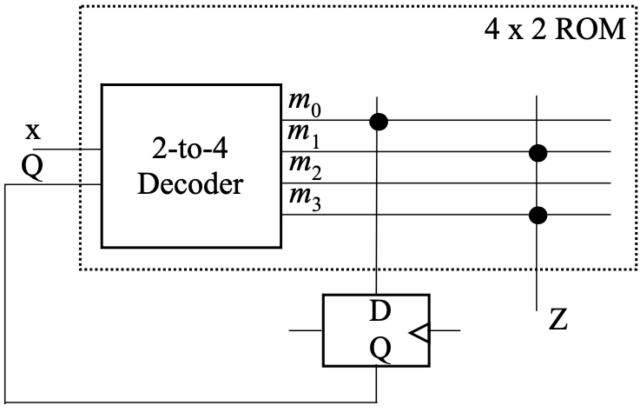

Fig. 2

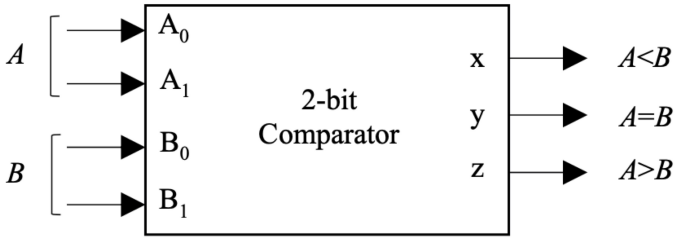

Fig. 3

3 (a) Discuss the technological difference between NMOS and CMOS logic. Provide at least two advantages of each of them. What is the key reason for the different size of the two fundamental elements of every CMOS circuit stage? Which important trade-off typically determines the operating voltage of microprocessors or similarly complex integrated circuits? [20%]

(b) Explain the key trade-off in NMOS when designing the electrical properties of basic components. How can each of the two necessary different components of an NMOS circuit be implemented specifically? [20%]

(c) Explain the key design difference between transistor–transistor and emitter-coupled logic? How do they compare performance-wise and what is the reason for the performance difference? [20%]

(d) Draw the typical circuit design of a one-transistor dynamic memory cell with address lines. Add the parasitic capacitances of the address lines. Which of those parasitic capacitances is most important for the signal integrity? Explain how this capacitance affects the signal. [10%]

(e) A complementary driver feeds a dynamic memory with a 1.2 V signal. The storage has a capacitance of 2 pF, the selection transistor has a $k = 10^{-5}$ A V^{-2} and is the key element determining the charging current. Each memory cell leaks with an equivalent resistance of 10^9 Ω.

(i) Calculate how long it takes to charge a cell from low to high level (10% to 90%)? Discuss whether that setup would allow writing the memory within a 600 MHz clock cycle? If not, explain which parameter of the transistor would need to change and by how much? [10%]

(ii) Calculate the dissipated power if the memory was operated at a 600 MHz clock and during every clock cycle two 64-bit words were written. Assume that 50% of all bits would flip during the writing procedure. [10%]

(iii) Calculate the dissipated power of one gigabit (i.e., 10^9 cells) just through leakage if on average half of the cells are in the high state. By how much would the dissipated power change if the voltage was at 3.3 V, which used to be a standard voltage for CMOS logic for many years and is still widely used in many embedded applications? [10%]

4 (a) The circuit given in Fig. 4 shows a logic gate. Which technology is used here? [10%]

(b) Calculate the values of R_1 and R_E assuring consistent logic levels for inputs and outputs. Use $V_{CC} = 0$ V, $V_{EE} = -6$ V, $V_R = -1.5$ V and a logic output swing of 1.2 V symmetrical around the reference voltage V_R. The base–emitter voltage is $V_{BE(on)} = 0.65$ V. The emitter currents should not exceed 4 mA. Set $R_2 = R_1$ for simplicity. (Hint: Assume that the base currents are negligible.) [30%]

(c) Draw a circuit compatible with the technology in Fig. 4 to generate a stable reference voltage V_R and explain briefly its principle of operation. How can diodes improve its performance? There is no need to provide any component values. [20%]

(d) Calculate the noise margins NM_H and NM_L. Derive V_{IH} and V_{IL} setting the width of the transition region of the voltage transfer characteristics to 150 mV, symmetrically around V_R. [20%]

(e) Draw a logically equivalent circuit to the one in Fig. 4 in CMOS technology. [20%]

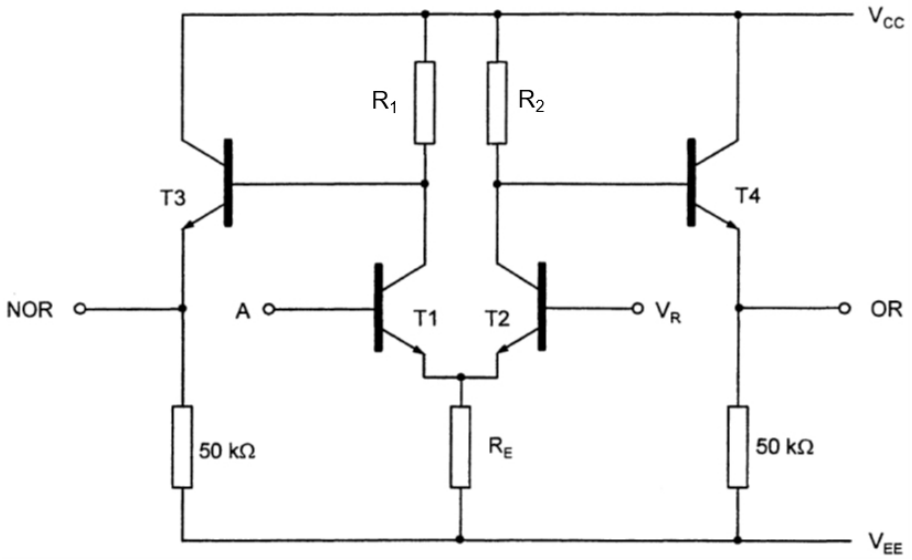

Fig. 4

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