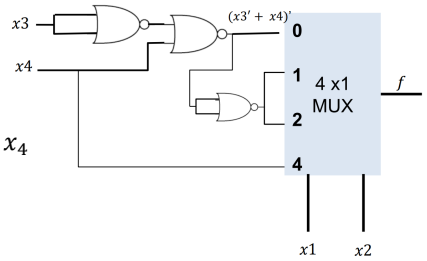
1 (a) Both CPLDs and FPGAs are based on logic blocks and programmable interconnects. However, CPLD's logic blocks contain multiple macrocells (typically 4 to 20) which provide product term arrays. FPGA's logic blocks are made of logic elements (LEs), which consist of lookup tables (LUTs), registers, etc. Compared to macrocells they are much more configurable and provide several extra features to improve performance and minimize wasted logic resources. For example, the LUT is key to the creation of product functions out of combinational logic in a FPGA. The LUT replaces the product term array found in CPLDs. FPGAs use 4 or more-input LUTs to create complicated functions. [20%]

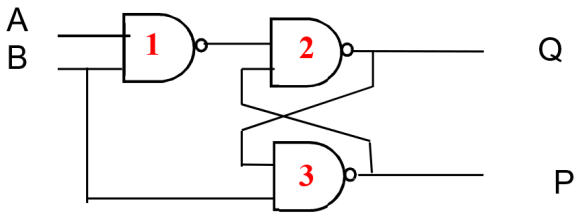
(b)

x_1	x_2	x_3	x_4	f	
0	0	0	0	0	
0	0	0	1	0	
0	0	1	0	1	$x_3x_4' = (x_3' + x_4)'$
0	0	1	1	0	
0	1	0	0	1	
0	1	0	1	1	
0	1	1	0	0	$(x_3x_4')' = x_3' + x_4$
0	1	1	1	1	
1	0	0	0	1	
1	0	0	1	1	
1	0	1	0	0	$(x_3x_4')' = x_3' + x_4$
1	0	1	1	1	
1	1	0	0	0	
1	1	0	1	1	
1	1	1	0	0	x_4
1	1	1	1	1	



[30%]

(c) (i)



A	B	Q	P	
0	0	0	1	If $B = 0$ then $P = 1$. The output of NAND1 is 1 and Q is 0 (stable).
0	1	0	1	After ($A = 0$, $B = 0$), $Q = 0$ from the previous state and $P = 1$. The output of NAND1 is 1 and $Q = 0$ (stable).
1	0	0	1	If $B = 0$ then $P = 1$. The output of NAND1 is 1 and Q is 0 (stable).
1	1	1	0	The output of NAND1 is 0. Therefore, the output of NAND2, $Q = 1$ and $P = 0$ (stable).
0	1	1	0	After ($A = 1$, $B = 1$), the output of NAND1 is 1. $P = 0$ from the previous state and $Q = 1$, $P = 0$ (stable).

A	B	
0	0	Reset
1	0	Reset
0	1	Don't change
1	1	Set

The circuit is stable and can be switched to another state and has set, reset, and don't change conditions. Therefore, it can be used as a memory unit. [30%]

(ii)

A	**B**	**Q(t)**	**Q(t+1)**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

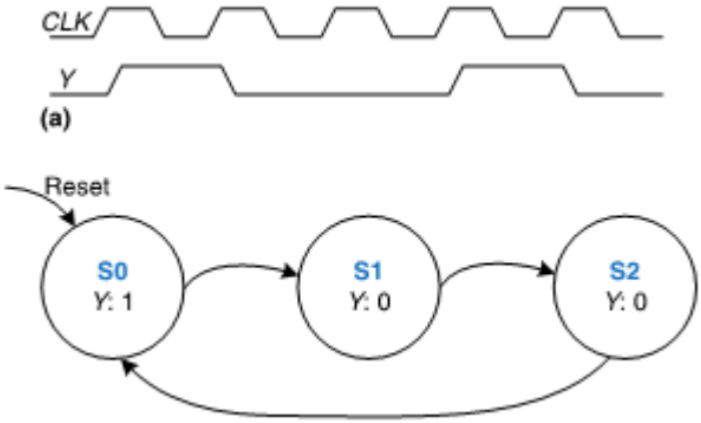
AB\Q(t)	**0**	**1**
00	0	0
01	0	1
11	1	1
10	0	0

Q(t+1) = BQ(t) + AB

(d) (i) The module describes the divide-by-3 counter. It provides a synchronous reset to initialize the FSM.

(ii) Divide-by-3 counter waveform and state transition diagram below where $S0 = 00$, $S1 = 01$, $S2 = 10$. The output Y is 1 when the state is 00 (i.e., $S0$):

(cont.



(iii) It is a a Moore machine. Because, the FSM has no inputs, only a clock and reset.

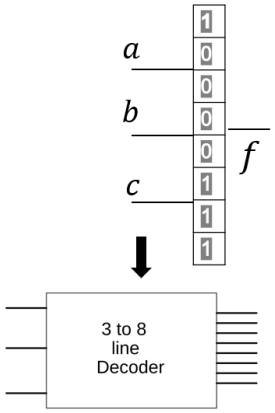
[20%]

2 (a) (i)

0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	1

[20%]

(ii)



$$f = c'b'a' + c(b'a + ba' + ba)$$
$$= c'(b'a') + c(b'a + ba' + ba).$$

Let $g = b'a'$.

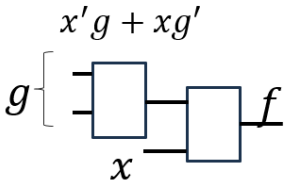
$$g' = (b'a')' = b + a$$

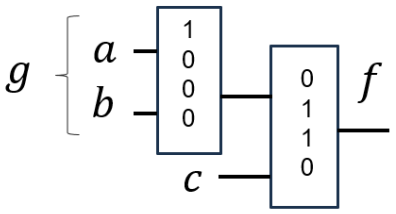
$$b + a = a(b' + b) + ba' = a + ba'$$

According to the absorption law: $a + ba' = a + b$. Hence,

$$f = c'g + cg$$

$f = c'g + cg'$ (XOR)





$a\ b$	$g = b'a'$
0 0	1
0 1	0
1 0	0
1 1	0

[30%]

(b) (i)

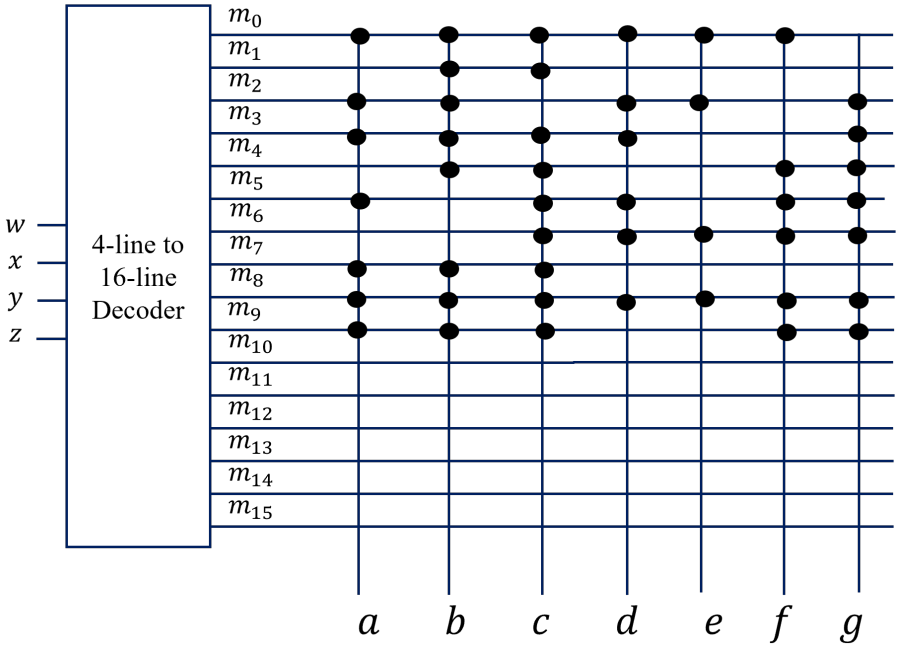
$w\ x\ y\ z$	$a\ b\ c\ d\ e\ f\ g$	Decimal number
0 0 0 0	1 1 1 1 1 1 0	0
0 0 0 1	0 1 1 0 0 0 0	1
0 0 1 0	1 1 0 1 1 0 1	2
0 0 1 1	1 1 1 1 0 0 1	3
0 1 0 0	0 1 1 0 0 1 1	4
0 1 0 1	1 0 1 1 0 1 1	5
0 1 1 0	0 0 1 1 1 1 1	6
0 1 1 1	1 1 1 0 0 0 0	7
1 0 0 0	1 1 1 1 1 1 1	8
1 0 0 1	1 1 1 0 0 1 1	9
1 0 1 0	X X X X X X X	
1 0 1 1	X X X X X X X	
1 1 0 0	X X X X X X X	
1 1 0 1	X X X X X X X	
1 1 1 0	X X X X X X X	
1 1 1 1	X X X X X X X	

$$a = w + xz + y\bar{x} + \bar{x}\bar{z}$$
$$b = w + \bar{x} + \bar{y}\bar{z} + yz$$

[20%]

(ii) Straightforward ROM implementation

(cont.



[20%]

A PLA can also be used. When the number of variables is small, a ROM is generally more economical than a PLA. However, when the number of input variables is large, PLAs often provide a more economical solution than ROMs. [20%]

(iii) 0, 8, 6, 9, 2, 2, 2, 1, 0 [10%]

3 (a)

The **low** state noise margin $\mathbf{NM_L = V_{IL} - V_{OL}}$

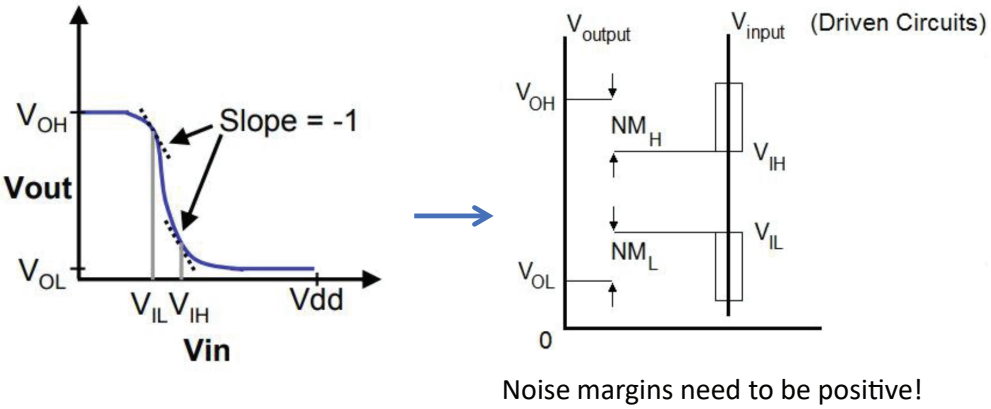
The **high** state noise margin $\mathbf{NM_H = V_{OH} - V_{IH}}$

$\mathbf{V_{OHA}}$ and $\mathbf{V_{OLA}}$ represent respectively:

- the lowest voltage supplied by logic circuit A delivering logic '1', and
- the highest voltage supplied by an output delivering logic '0'

$\mathbf{V_{IHB}}$ and $\mathbf{V_{ILB}}$ represent respectively:

- the lowest input to B acceptable as logic '1'
- the highest input to B acceptable as logic '0'



[10%]

(b) The noise margin describes by how much the worst-case output of one stage may fluctuate due to noise or be distorted by interference before its output is not reliably identified as the correct logic level anymore by the next stage.

This becomes particularly important when different logic families are combined, which practically happens every times an IC is connected with some peripheral electronics or other ICs. [10%]

(c) Transistors switch rather rapidly once the gate-source voltage exceeds their threshold ($\pm 0.5V$). Thus, the logic limits are 0.5 V and 1.1 V − 0.5 V = 0.6 V. [15%]

(d)

Case 1: V_{in} = 0 V
nMOS off as $V_{in} << V_{th,n}$ = 0.5 V
pMOS on as $V_{in} << V_{CC} - V_{th,p}$ = 0.6 V, linear as $V_{ds} = V_{OH} - V_{CC} \rightarrow 0$ V
$\Rightarrow$ output at $V_{OH} = V_{CC}$ = 1.1 V

Case 2: V_{in} = 1.1 V
nMOS on as $V_{in} >> V_{th,n}$ = 0.5 V
pMOS off as $V_{in} >> V_{CC} - V_{th,p}$ = 0.6 V, linear as $V_{ds} = V_{OH} \rightarrow 0$ V
$\Rightarrow$ output at V_{OL} = 0 V

Case 3: V_{in} = 0.55 V
nMOS on as $V_{gs} > V_{th,n}$ = 0.5 V

(cont.

pMOS on as $V_{gs} = V_{in} - V_{CC} = 0.55\ \text{V} - 1.1\ \text{V} = -0.55\ \text{V} < V_{th,p} = -0.5\ \text{V}$
Both same transconductance so that problem symmetric:
$V_{out} = V_{CC}/2 = 0.55\ \text{V}$
$\Rightarrow V_{ds,n} = 0.55\ \text{V} > V_{gs,n} - V_{th,n} = 0.55\ \text{V} - 0.5\ \text{V} = 0.05\ \text{V}$
p transistor equivalent due to symmetry $\Rightarrow$ both transistors saturated

[20%]

(e)

$\mathbf{NM_L} = \mathbf{V_{IL}} - \mathbf{V_{OL}} = 0.5\ \text{V} - 0\ \text{V} = 0.5\ \text{V}$
$\mathbf{NM_H} = \mathbf{V_{OH}} - \mathbf{V_{IH}} = 1.1\ \text{V} - 0.6\ \text{V} = 0.5\ \text{V}$

[10%]

(f) 90% to 10% fall time of an inverter means that the low-side n-type field-effect transistor has to discharge the output capacitance. Simplifying the transistor and other limiting elements to an equivalent resistor, the discharge process is approximately an exponential decay.

$$V(t) \approx V_0 \,.\, \exp\left(-\frac{t}{RC}\right)$$

$$t_{90-10} = t_{90} - t_{10} = -RC(\ln 0.9 - \ln 0.1) \approx 2.2RC$$

Estimate R, e.g., from approximately half the gate-source voltage throughout the process:

$$R \approx \frac{1}{k\left(\frac{V_{CC}}{2} - V_{th}\right)}$$

[20%]

(g)

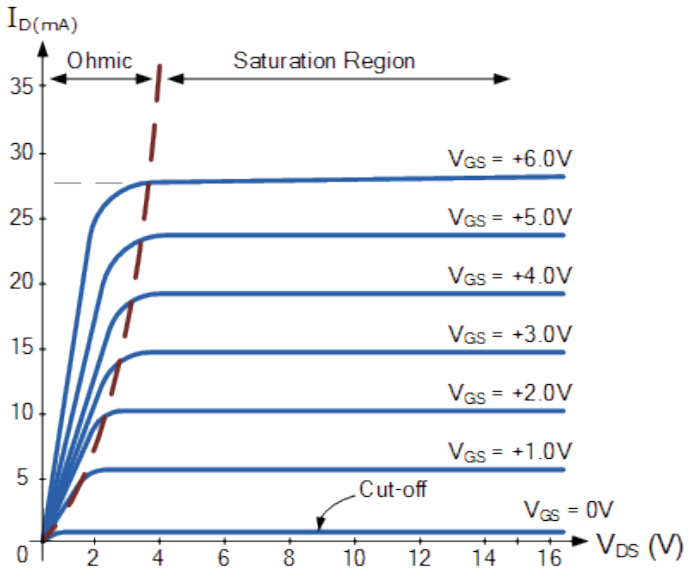
$$R \approx \frac{1}{10^{-5}\frac{\text{A}}{\text{V}^2}(0.55\ \text{V} - 0.5\ \text{V})} = 2\ \ \text{M}\Omega$$

$$t_{90-10} \approx 2\ \text{M}\Omega\ .\ 2\ \text{pF} = 4\ \mu\text{s}$$

Similar approximations of R with the same order of magnitude also fine.

[15%]

4 (a) For field-effect transistors, saturation refers to the channel. For the provided gate-source voltage, the maximum current is reached, and a higher drain-source voltage will not further increase the channel current. The reason can be the channel pinching off near the drain or a saturation of the charge carrier speed. In logic transistors, this saturation effect is typically associated with the channel pinched off at the drain side as the gate-drain voltage is not strong enough to attract sufficient charge carrier densities in this region locally anymore. (Optional: Short-channel effects can ease saturation to some degree.) The condition for saturation of an n-channel field-effect transistor is $V_{ds} > V_{gs} - V_{th}$. As the current is practically constant in saturation even if the drain-source voltage is increased, the transistor behaves as a constant-current source from that point onwards. This behaviour is useful, e.g., if field-effect transistors are to be used as resistors with the gate connected to drain, which then fulfils the above condition for saturation and allows forming larger resistance values than if the transistor were in the linear range. Furthermore, saturation limits the power losses, e.g., during transitions in complementary MOS technology, where channel saturation limits the shunted current across the pmos-nmos gates from supply to ground.



For bipolar transistors saturation refers to the effect that the base is flooded with so many charge carriers (as the base–emitter loop has hardly any resistance once the voltage exceeds the typical pn voltage) that the collector-emitter current is no longer following

(cont.

proportionally (gain drops). The background is as follows: The collector–emitter voltage falls to a relatively constant $V_{ce,sat}$ level, which is typically provided by manufacturers and around 1/3 of the base-emitter voltage. As a consequence, the base-collector pn junction becomes forward-biased so that the base-collector current loop injects a large quantity of charge carriers so that the carrier density in the base exceeds normal levels. These charge carriers become noticeable when the transistor is supposed to be turned off again. The base excess charge can then only vanish through diffusion and recombination.

The major problem of saturation in bipolar transistors is the speed limitation it causes in logic families that saturate bipolar transistors. Saturation can be limited by adding a Schottky shunting diode from the base to the collector to guide the excess current through the collector rather than the base in case the base potential exceeds the collector potential.

On the other hand, $V_{ce,sat}$ is a relatively stable voltage level and can be used as a voltage level. [20%]

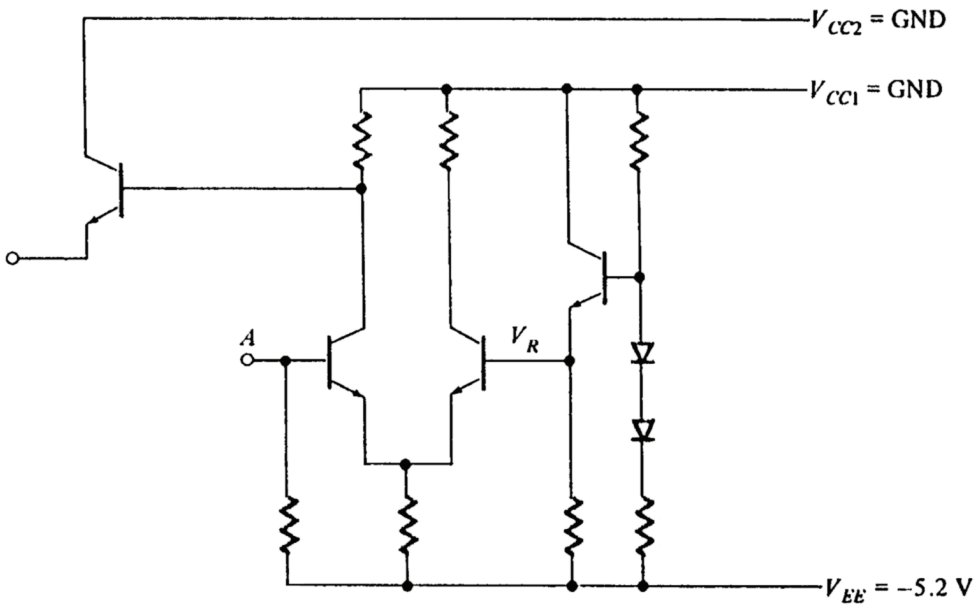
(b) Logic classes with saturation problem:
(bipolar) transistor–transistor logic (TTL), (bipolar) transistor–resistor logic (TRL)

Mitigation strategies:

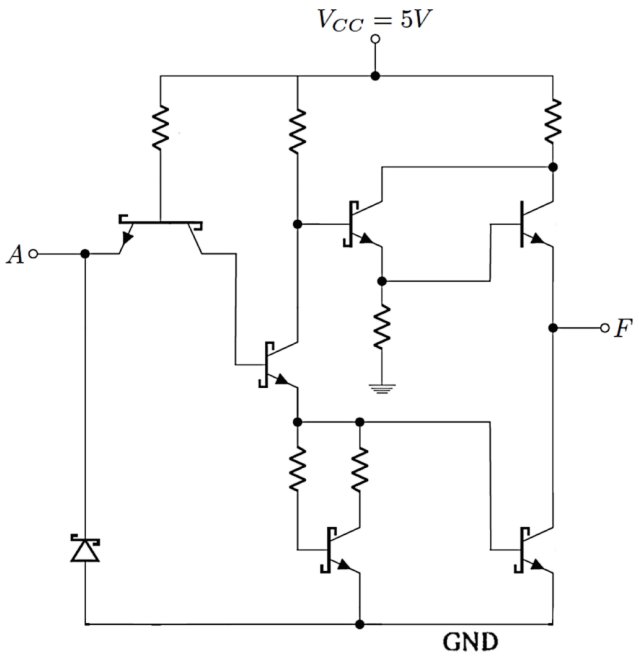
(i) Parallel Schottky junction from the base to the collector to avoid feeding excess charge into the base (Schottky TTL and low-power Schottky TTL). Schottky (metal-semiconductor) junction instead of pn junction for lower forward voltage so that less current flows through the base. When transistor is to be turned off, less excess charge, which has to recombine (or diffuse away) is available, which would keep the device on longer otherwise.

(ii) Emitter-coupled logic (ECL) does not use transistors as voltage-level switch through hard switching into saturation but uses differential pairs (as in operational amplifiers or comparators) and operates them exclusively in the linear (cut-off) range. The transistors are operated as current amplifiers and shift the balance between two branches with (relatively) constant and limited current sum. Without saturation, the transition between logic levels is fast. [10%]

(c) ECL Inverter



Schotty TTL Inverter



[20%]

 (cont.

(d)

NMOS: network of n-type field-effect transistors (FETs) operate against a resistor. Basic structure: positive supply → resistor → series-parallel configuration of several n-type field-effect transistors → ground. The output is the node between the resistor and the transistor network. Thus, the needed components in this technology are n-type field-effect transistors and resistors. The latter can be implemented by long meandering conductor traces (e.g., poly-Si, but hard to achieve sufficient resistance values with that) or field-effect transistors (for NMOS typically also n-type) with the gate hard-wired to the drain so that the transistor is forced into saturation.

As only one type of transistor is needed, manufacturing needs fewer process steps and is cheaper therefore. However, if the output is low, there is constant current flowing from the supply through the resistor and the transistor network, which is pulling the output down. Constant loss in this state is the consequence. Furthermore, switching the output from high to low is active through transistors and fast. Switching from low to high requires pulling up the output through the resistor, which should be large enough for moderate static power loss. Accordingly, at least one transition tends to be rather slow. The selection of the resistor value, typically through the selection of the channel width of the n-FET that represents it, is a trade-off between speed and static power loss. The narrowest channel is typically given by the lithography of the process. Space-wise, only one resistor is needed. For complex gates, NMOS is more compact than CMOS as NMOS only needs one pull-up resistor. CMOS in contrast mirrors the n-network in the p-network, which consequently has similarly many transistors as the n-network.

CMOS: a high-side p-network operates against a matched complementary low-side n-network. Complementary means that every transistor in the n-network has a partner in the p-network and series and parallel configurations swap.

Structure: Positive supply → p-network → n-network → ground. The output is between the complementary networks.

The output is actively pulled up and down so that both can be similarly fast. p-type transistors have typically higher resistance for the same size (mobility of holes as low as half of that of electrons in silicon). Therefore, for similar low-to-high and high-to-low transition times of the output, the transistors in the p-network have to be made wider. The

exact ratio depends on the specific gate. In an inverter it would be about twice as wide. In a NAND gate, p vs. n width of the transistors is closer in size to each other (almost 1:1) as two series low-side NMOS have round about the resistance of one of the two parallel PMOS pulling the output high.

CMOS is typically faster, has practically no static power loss (not considering leakage and static parasitics in modern transistors), but needs more processing steps (additional doping for contacts, wells, etc.) and related masks and is therefore more expensive (both fixed and variable cost). Due to lower loss (heating) and higher speed, it is still by far the most widely used integrated logic technology right now. [15%]

(e) Resistor could be implemented as long conductive path, e.g., of poly-silicon, which would be widely linear as used from resistors. Alternatively, a field-effect transistor with its gate connected to drain can be forced into saturation so that the typical squared relationship

$$I_d = \frac{k}{2}\frac{W}{L}(V_{\text{gs}} - V_{\text{th}})^2$$

applies. Thus, this kind of resistor representation is not linear, but the current rises stronger than in the ohmic case. Thus, over-proportionally more current flows for higher voltages across the transistor.

Overall, the resistor representation as a saturated field-effect transistor is notably smaller (easily a decimal order of magnitude) than through a conductor path for the resistance range needed in NMOS. [10%]

(f) The stronger-than-linear growth of current in saturated transistors is not ideal for NMOS circuits as that means that when the low-side network forms some conductive path and pulls the output low, the high-side resistor representation even conducts more then necessary, and this current is entirely power loss. A resistor with less than linear current-voltage relationship would be ideal in that case, but does not exist as a viable solution. [15%]

(g) CMOS is by far dominant in the integrated logic market and latest processors. However, already now, the structures cannot easily be reduced in size anymore as was the case in the decades before. Lithography techniques are hitting walls, and transistors with extremely short channels do not large on/off modulation (on-current vs. leakage) anymore. FinFETs and Gate-all-around (GAA) transistors modulate the channel from several sides

(therefore also considered 3D processes) for a stronger on/off ratio.

Second, heat is a problem or more accurately the loss-power density. Due to the squared influence of the supply voltage on the losses, transistors and circuits are designed for lower and lower voltages ($\ll 1V$), which means that also the threshold voltage has to be decreased. [10%]

END OF PAPER

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