Version OBA/2

EGT2
ENGINEERING TRIPOS PART IIA

Monday 06 May 2024 14.00 to 15.40

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS

Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM

CUED approved calculator allowed

Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 (a) Explain the differences between Complex Programmable Logic Devices (CPLDs) and Field-Programmable Gate Arrays (FPGAs). [10%]

(b) Implement a 4-variable Boolean function:

$$f(x_1, x_2, x_3, x_4) = \sum (2, 4, 5, 7, 8, 9, 11, 13, 15)$$

using a single 4-to-1 multiplexer and minimal number of two-input NOR gates. Use x_1 and x_2 as select input lines in the multiplexer. Use only variables x_1, x_2, x_3, x_4 as inputs (not their complements). [30%]

(c) (i) Analyse the circuit depicted in Fig. 1 by applying different input values and demonstrate that this circuit can function as a memory unit. [20%]

(ii) Derive the next state equation for Q as $Q(t + 1) = f(A, B, Q(t))$. [20%]

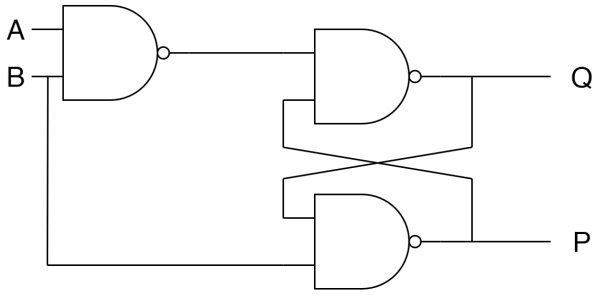

Fig. 1

(d) (i) Consider the VHDL code in Fig. 2. What does the logic circuit implemented by this code do? Explain your answer. [5%]

(ii) Draw the output waveform of the circuit implemented by this VHDL code in response to the clock signal. [5%]

(iii) Draw the state diagram for the circuit implemented by this code. Clarify the condition under which the output is set to 1. [5%]

(iv) Determine whether this logic circuit is a Mealy or Moore machine. Explain your answer. [5%]

(cont.

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity customFSM is
 port(clk, reset: in STD_LOGIC;
      y: out STD_LOGIC);
end;

architecture synth of customFSM is
 signal state, nextstate:
 STD_LOGIC_VECTOR(1 downto 0);
 begin
  process(clk) begin
   if clk'event and clk = '1' then
    if reset = '1' then state <= "00";
    else state <= nextstate;
    end if;
   end if;
  end process;
 nextstate <= "01" when state = "00" else
              "10" when state = "01" else
              "00";
 y <= '1' when state = "00" else '0';
 end;
```

Fig. 2

2 (a) Fig. 3 shows the circuit for a 4-LUT.

(i) Find the storage cell contents needed to implement the function: [20%]

$$f = x_0x_1 + \bar{x_0}\bar{x_1}x_2x_3$$

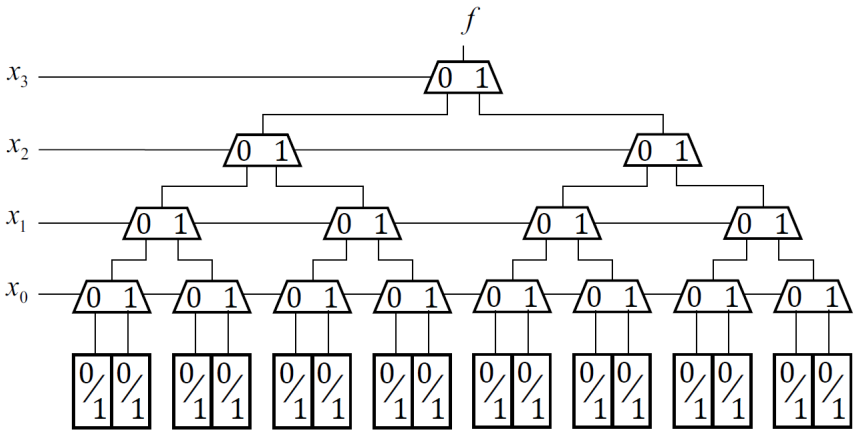

Fig. 3

(ii) Implement the logic function $f(a, b, c) = \Sigma(0, 5, 6, 7)$ using two 2-LUTs. [30%]

(b) Fig. 4(a) shows the circuit for a BCD-to-7-segment display decoder, with w the Most Significant Bit (MSB).

(i) Build the truth table and find the output functions for a and b. [20%]

(ii) Implement the circuit using ROM and discuss the advantages and disadvantages compared to its implementation with PLA. [20%]

(iii) If the waveforms shown in Fig. 4(b) are applied to the decoder input, determine the sequence of digits that appears on the display. [10%]

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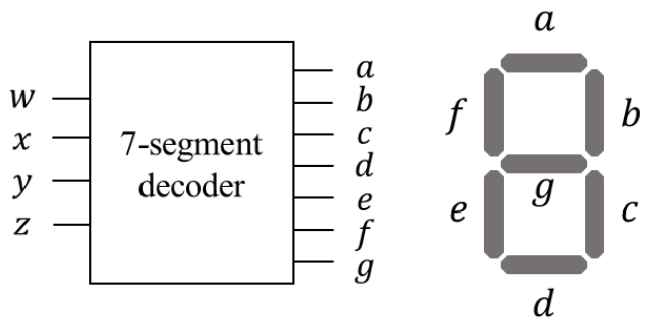
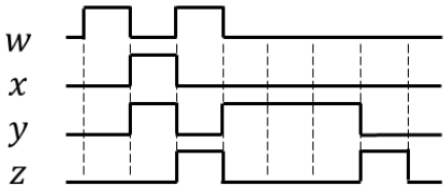


(a)



(b)

Fig. 4

3 A CMOS inverter inside a larger integrated circuit is operated at 1.1 V supply voltage. The inverter uses two transistors, each with a transconductance $k = 10^{-5}$ A/V^2, and the threshold voltages of the transistors are respectively +0.5 V and −0.5 V. The output stage is loaded with further logical circuits, summarised through their effective capacitance $C_\mathrm{L} = 2$ pF. On the output side, low logic levels should be below 0.3 V, high levels above 0.7 V.

(a) Explain graphically with the transfer characteristics of the inverter, how to derive the noise margin. [10%]

(b) What does the noise margin describe and in which situations is it important? [10%]

(c) Approximate the input thresholds for high and low levels. [15%]

(d) Calculate the output levels for 0 V, 0.55 V, and 1.1 V input. In which mode are the individual transistors in each condition? [20%]

(e) Calculate the noise margins. [10%]

(f) Derive an expression for the 90% – 10% fall time in response to an abrupt rising voltage step at the input. You may substantially simplify the expression if all necessary assumptions are given. [20%]

(g) Determine the 90% – 10% fall time. [15%]

Current of a field-effect transistor:

$$I_\mathrm{D} = k\left((V_\mathrm{GS} - V_\mathrm{T})V_\mathrm{DS} - \frac{V_\mathrm{DS}^2}{2}\right) \quad \text{for } V_\mathrm{DS} < V_\mathrm{GS} - V_\mathrm{T} \text{ and}$$

$$I_\mathrm{D} = \frac{k}{2}(V_\mathrm{GS} - V_\mathrm{T})^2 \qquad \text{for } V_\mathrm{DS} \geq V_\mathrm{GS} - V_\mathrm{T}$$

4 (a) Explain the difference between saturation of a bipolar junction transistor and of a field-effect transistor (FET). Indicate which part of the transistor saturates in each case and how it affects the currents of the three contacts of the specific transistor. Mark the effect in the voltage–current characteristics plot of field-effect transistors. How does saturation of bipolar and field-effect transistors affect logic circuits? [20%]

(b) List one logic circuit where saturation of transistors is a problem. Which logic classes can be used to overcome this saturation problem? Further explain briefly how the problems of saturation are avoided by these alternatives. [10%]

(c) Sketch inverter circuits for one logic circuit family that avoids saturation. [20%]

(d) Compare NMOS and CMOS logic with respect to circuit structure, required elements, speed, power consumption, and necessary manufacturing steps. How are the high-side and low-side sub-circuits of a gate matched in NMOS and CMOS? Take the example of a NAND gate. Briefly name any trade-offs and the involved metrics that may influence this matching. [15%]

(e) Briefly discuss the alternatives for implementing resistors on integrated circuits with respect to size and linearity. [10%]

(f) In which logic circuit class does the linearity of a resistor matter and in what way? Would this circuit class rather benefit from stronger than linear growth of the current with voltage or from a lower than linear growth? [15%]

(g) Which logic class is used in most of the recent microprocessors and digital integrated circuits? Major performance gains in these chips depended on exponential size reduction of transistors in previous decades. Which two problems does the further size reduction cause? Which recent transistor technologies do try to solve these problems and how? [10%]

END OF PAPER

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