Version OBA/2

EGT2
ENGINEERING TRIPOS PART IIA

Friday 2 May 2025 09.30 to 11.10

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS

Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM

CUED approved calculator allowed

Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 (a) Use Shannon's expansion to find the canonical sum-of-products (SOP) form of the function $f = x_2 + \overline{x_1}\,\overline{x_3}$. [15%]

Solution:

Expansion in terms of x_1 gives:

$$f = \overline{x_1}x_2 + \overline{x_1x_3} + x_1x_2$$

Further expansion in terms of x_2 gives:

$$f = \overline{x_2}\,(\overline{x_1x_3}) + x_2(x_1 + \overline{x_1} + \overline{x_1x_3})$$
$$= \overline{x_1}x_2 + \overline{x_1}x_2\overline{x_3} + \overline{x_1x_2x_3} + x_1x_2$$

Further expansion in terms of x_3 gives:

$$f = \overline{x_3}\,(\overline{x_1x_2} + x_1x_2 + \overline{x_1}x_2 + \overline{x_1}x_2) + x_3(x_1x_2 + \overline{x_1}x_2)$$
$$= \overline{x_1x_2x_3} + x_1x_2\overline{x_3} + \overline{x_1}x_2\overline{x_3} + \overline{x_1}x_2x_3 + x_1x_2x_3$$

(b) Specify the size of a ROM that you could use to program the following two combinational circuits:

(i) An 8-bit adder/subtractor with C_{IN} and C_{OUT}. [5%]

Solution:
Number of inputs = 2x8+1=17
Number of outputs = 8+1=9
Hence, this would require $2^{17}x9$ - bit ROM

(ii) An 8×8 multiplier. [5%]

Solution:
Number of inputs = 16
Number of outputs = 16
Hence, this would require $2^{16}x16$ - bit ROM

(iii) Is using a ROM to implement the functions in part (b) (i) and (ii) a good design choice? Explain why or why not. [5%]

Solution:
These implementations are not good design choices. They could be implemented in a smaller amount of hardware using discrete gates.

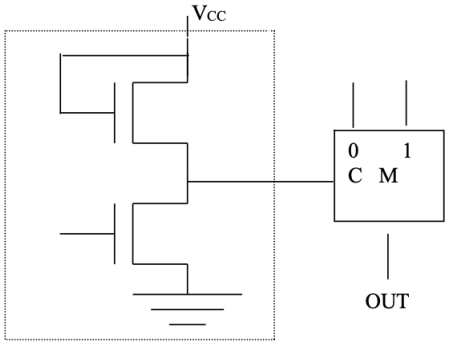
(cont.

(c) A macro-cell, part of a complex combinational/sequential Programmable Array Logic (PAL) has been programmed as shown in Fig. 1. The binary gate signals on the *n*-channel MOSFET switches, G1 and G2, control the 2-1 multiplexers and the non-inverting tri-state buffers B1, B2, and B3. There are two main inputs labelled *X* and *Y* and one output labelled O1. The I/O2 pin can operate either as an extra input or the second output of the macro-cell. The bistable is of J-K type.

(i) Describe the multiple operations of the macro-cell and find the logic functions for all combinations of the gate signals G1 and G2. [30%]

Solution:

(i) The control circuits connected to M_1 and M_2 are NMOS inverters.



NMOS INVERTER

- **If $G_1 = 1 \Rightarrow C_1 = 0 \Rightarrow I/O_2$** is configured as input, $I/O_2 = I$. The input I is selected at the M_1 multiplexer and becomes (or not) an input in the PAL function of the signal G2.
  - **$G_2 = 1 \Rightarrow C_2 = 0$**, B3 is open circuit and therefore
    $O_1 = \overline{X}\,\overline{Y} + \overline{X}Y + \overline{Y}X + XY = 1$
  - **$G_2 = 1 \Rightarrow C_2 = 1$** In this case the macro-cell behaves as a single output combinational circuit with 3 inputs X, Y, I. The logic function implemented is that of binary adder (with no carry):
    $O_1 = \overline{X}\,\overline{Y}I + \overline{X}I\overline{Y} + I\overline{Y}X + XYI = X \oplus Y \oplus I$

- **If $G_1 = 0$ and $G_2 = 1 \Rightarrow C_1 = 1, C_2 = 0$**

B_2 and B_3 are inactive (open circuit) and $I/O_2 = O_2$.
The bistable is bypassed and the macro-cell behaves as a two output combinational network with two inputs.

$$\begin{cases} O_1 = \overline{X}\,\overline{Y} + \overline{X}Y + \overline{Y}X + XY = 1 \\ O_2 = XY \end{cases}$$

- **If $G_1 = 0$ and $G_2 = 0 \Rightarrow C_1 = 1, C_2 = 1$**

B_1, B_2 and B_3 are shortcircuits, M_1 and M_2 select the input "1". The cell behaves as a MEALY sequential circuit (as the output depends on both the present state and the primary inputs). There are two outputs O_1 and O_2. The inputs to the bistable JK are:

$J = XY$ $\qquad$ $K = \overline{X}\,\overline{Y}$

(ii) Derive the state diagram if the macro-cell is operated as a state-machine. What type of architecture is the state-machine? [20%]

Solution:

(ii) *Using the JQ bistable equation and the* reverse method we can work out Q^+ and the inputs to the bistable, J and K.

$$Q+ = \overline{Q}J + Q\overline{K} = \overline{Q}XY + Q(X+Y)$$

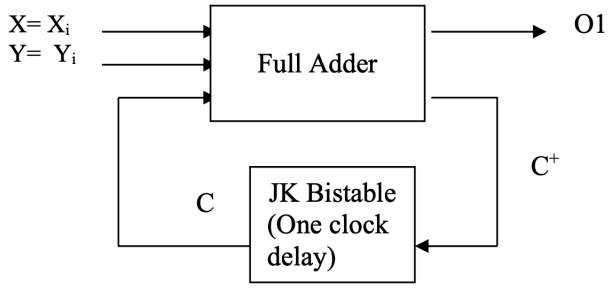
$$O1 = X \oplus Y \oplus Q$$

XY	**Q**	Output O1	Next state Q^+	JK
00	0	0	0	0x
00	1	1	0	x1
01	0	1	0	0x
01	1	0	1	x0
10	0	1	0	0x
10	1	0	1	x0
11	0	0	1	1x
11	1	1	1	x0

(iii) Consider that the macro-cell is operated as a state-machine and only output O1 is of interest. Draw a simplified block diagram of the circuit. What specific function does the circuit perform? [20%]

Solution:

(iii) This is a serial binary adder. The XY are the inputs Xi Yi (serially entered). Q is the Carry. Q+ is the C+ and O1 is the output (the sum)



C = carry bit (present state)
C^+ = next carry bit (next state)

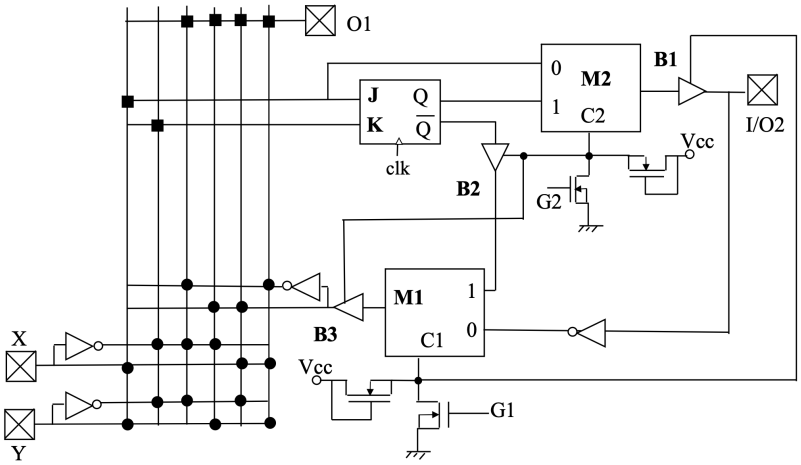


Fig. 1

2 (a) Compare and discuss EPROM, EEPROM and SRAM programming technologies. [20%]

Solution:

EPROM and EEPROM are non-volatile memories, i.e. can retrieve stored information even after having been turned off and back on. This is the opposite of SRAM (volatile memory) which needs constant power to prevent data from being erased. EPROMs can be reprogrammed by using UV light, in comparison to EEPROMs, which can be electrically reprogrammed.

(b) In order to automate its storage facilities, a warehouse has decided to design the sorting conveyor system shown in Fig. 2. The sorter controller can detect the length of incoming boxes (to be stored) and divert only the ones that are long. For simplicity, you may assume that all boxes are of only two sizes, either small or big. Using two sensors (S_1 and S_2), the small boxes will never pass under both sensors at one time, however, the big ones will. The sensor input will be set to logic high when a box is under the sensor; otherwise, it will remain at zero. After a big box is detected (i.e., the end of the box passes sensor S_2), the sorter must be activated, which will divert the box to the second output. You may also assume that there will always be sufficient space between boxes such that two boxes will never be under the sensors at the same time.

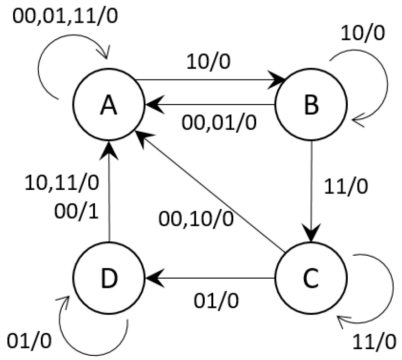
For all input sequences that are not physically possible, it needs to be ensured that the system returns to the initial state. Furthermore, all unused states should return the system to the initial state.

(i) Design the digital circuit for the sorter controller shown in Fig. 2. Draw the state diagram and the state table. [40%]

Solution:

(cont.

(b) (i)

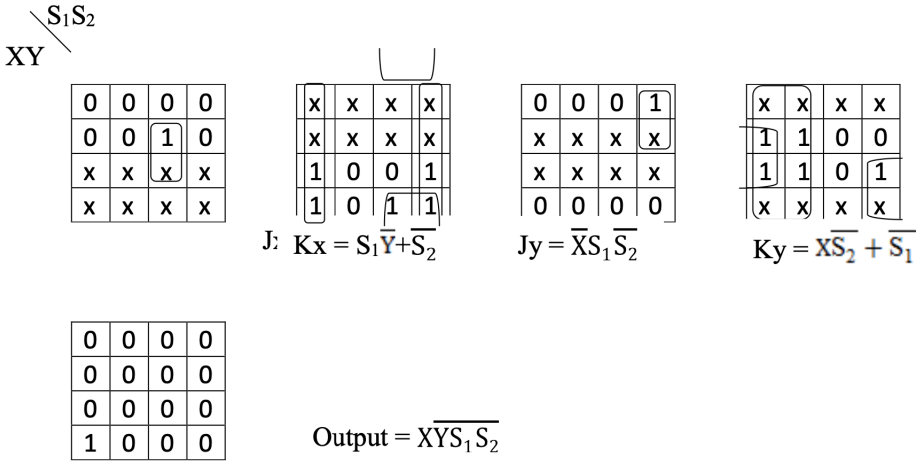


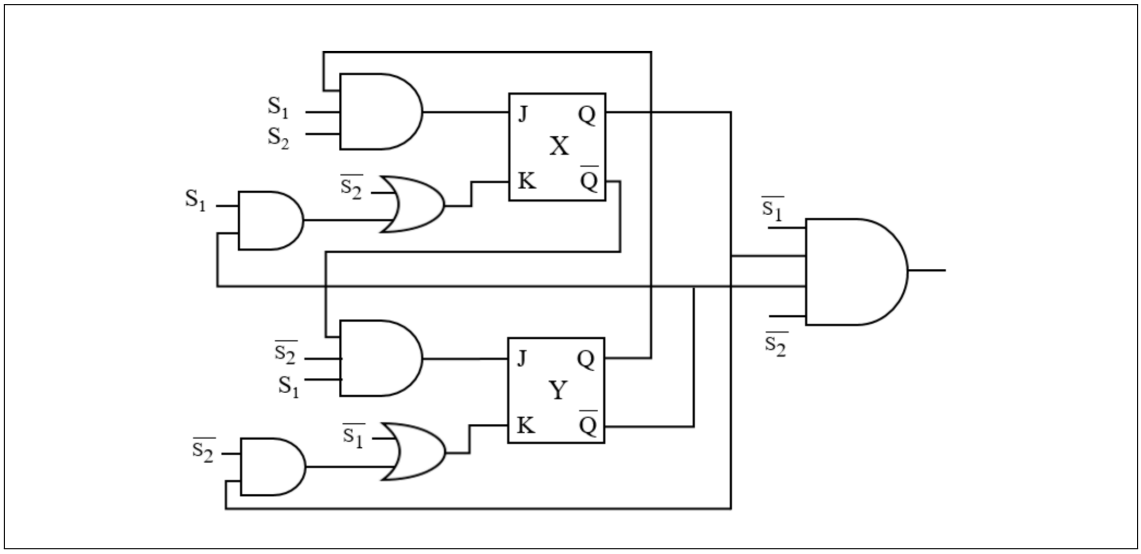
Present state		Next state for S_1S_2				Bistable inputs for S_1S_2 = JxKx				Bistable inputs for S_1S_2 = JyKy				Output			
	XY	00	01	11	10	00	01	11	10	00	01	11	10	00	01	11	10
A	00	00	00	00	01	0x	0x	0x	0x	0x	0x	0x	1x	0	0	0	0
B	01	00	00	11	01	0x	0x	1x	0x	x1	x1	x0	x0	0	0	0	0
C	11	00	10	11	00	x1	x0	x0	x1	x1	x1	x0	x1	0	0	0	0
D	10	00	10	00	00	x1	x0	x1	x1	0x	0x	0x	0x	1	0	0	0

(ii) Draw the circuit implementation of the controller using J-K bistables and logic gates. [20%]

Solution:

(ii)



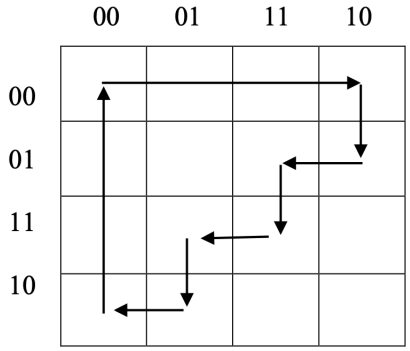


(iii) Comment on the existence of hazards, if any, in the implemented circuit. [20%]

Solution:

(iii) The feedback from X and Y is delayed by few 10s ns. S_1 and S_2 cannot change that quickly since there is a considerable distance between the two detectors.

Only one bit changes at one time in the combined S_1S_2XY.



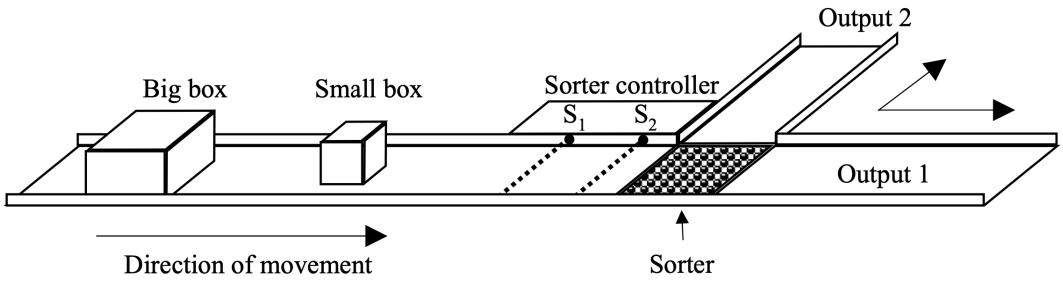


Fig. 2

3 (a) A microprocessor manufactured in 1996 operates at a rate of 10^6 calculations per second. Explain what rate of calculations you would expect from a microprocessor of the same price that has been manufactured four to five years later. [15%]

Solution:

According to Moore's law, semiconductor technology doubles its capability every 18 months to two years.

Therefore in 4 years' time, the microprocessor should manage $2^2 - 2^{2.5}$ times speed up over 10^6 (i.e. 4-5.6$\times 10^6$) operations per second per £x.

(b) NMOS inverters, which were popular before CMOS inverters, use a resistor to pull up the output. Explain briefly a drawback of NMOS inverters. [10%]

Solution:

Small low noise margin: the NMOS transistor is turned ON once the input voltage is over its threshold $V_t = 0.43$. V_o will start to fall and as a result the low noise margin is as little as 0.43 V.

OR

Static power dissipation: when the inverter's output is low, the NMOS transistor is ON and there will be a short-circuit current from V_{cc} to ground. This increases the (static) power dissipation of the inverter.

(c) A CMOS inverter is shown in Fig. 3. It is operated at a supply voltage of 2.5 V and is manufactured in a 0.25 μm process technology with the following parameters:

	NMOS	PMOS
Threshold voltage V_t (V)	0.43	−0.4
k' (μA/V^2)	115	−30

Assume that there is only capacitive load C_L at the output.

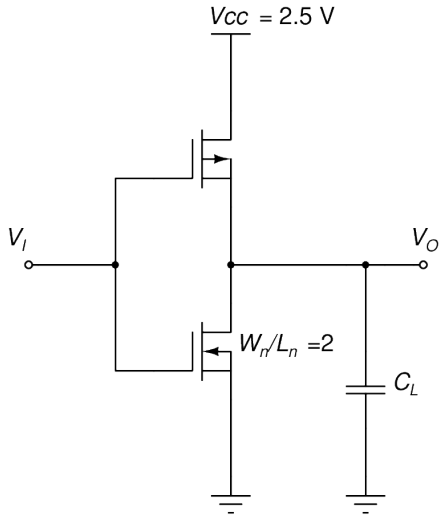


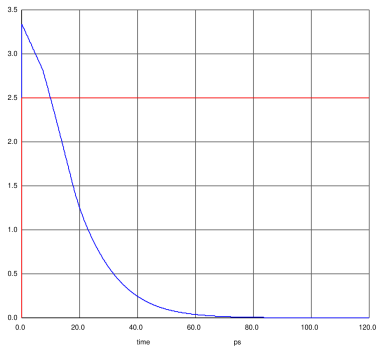
Fig. 3

(i) What would be the low output voltage V_{OL} of the inverter? Explain briefly the mode of operation of the NMOS transistor when V_O is close to V_{OL}. [15%]

Solution:
V_{OL} is 0 V.
For NMOS transistor, $V_{GS} = V_{cc} = 2.5V$, $V_{DS} \approx 0 < V_{GS} - V_t$ so it is in linear region/mode.

(ii) Suppose a step input from 0 to 2.5 V is supplied to V_I at time $t = 0$. Sketch the change of V_O, which is initially 2.5 V, with respect to time. [10%]

Solution:



Red: step input; blue: change of V_O with time t.
Note: The clock feedthrough may be omitted in the answer.

(cont.

(iii) What width-to-length ratio (W_p/L_p) for the PMOS transistor would make $V_I = V_O = 1.25$ V? You may make use of the fact that $|I_{Dp}| = |I_{Dn}|$. Ignore channel length modulation (i.e., $\lambda = 0$). [25%]

Solution:
Both transistors are in saturation when $V_I = V_O = 1.25$ V.

$$I_{Dn} = (\frac{115}{2})(2)(1.25 - 0.43)^2 = 77.3 \quad \mu\text{A}$$
$$|I_{Dp}| = (\frac{30}{2})(\frac{W_p}{L_p})(1.25 - 0.4)^2 = 10.8(\frac{W_p}{L_p}) \quad \mu\text{A}$$
$$|I_{Dp}| = |I_{Dn}|$$
$$10.8(\frac{W_p}{L_p}) = 77.3$$
$$\frac{W_p}{L_p} = 7.14$$

(iv) If the switching speed of the inverter has to be further increased, what change(s) would you suggest and why? [15%]

Solution:
The width-to-length ratios should be increased such that the transistors can provide more currents in charging and discharging capacitances during switches. That reduces the equivalent resistances of the transistors.

The following current equations of a field-effect transistor may be useful:

$$k = k' \cdot \frac{W}{L}$$
$$I_D = k\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right) \qquad \text{for} \quad V_{DS} < V_{GS} - V_T$$
$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \qquad \text{for} \quad V_{DS} \geq V_{GS} - V_T$$

(d) Suggest a new kind of transistor technology that could replace CMOS technology in the near future. State an advantage of this new kind of transistor technology. [10%]

Solution:

Any of the following:

- Thin-Body MOSFETs: Off-state leakage is suppressed by using an adequately thin body region, which may be eliminated entirely.
- FinFETs: the 3D structure reduces leakage.
- Graphene FETs: High charge carrier mobility and saturation velocity

4 A design of a transistor-transistor logic (TTL) 2-input NAND gate is shown in Fig. 4. The supply voltage V_{cc} is 5 V and all resistance values are provided in Ohm (Ω). Assume that the diode on-state voltage is 0.7 V, the transistor on-state base-emitter voltage and the saturated transistor collector-emitter voltage are 0.7 V and 0.2 V, respectively. The forward gain β_F is 50, and the reverse gain β_R is 0.1.

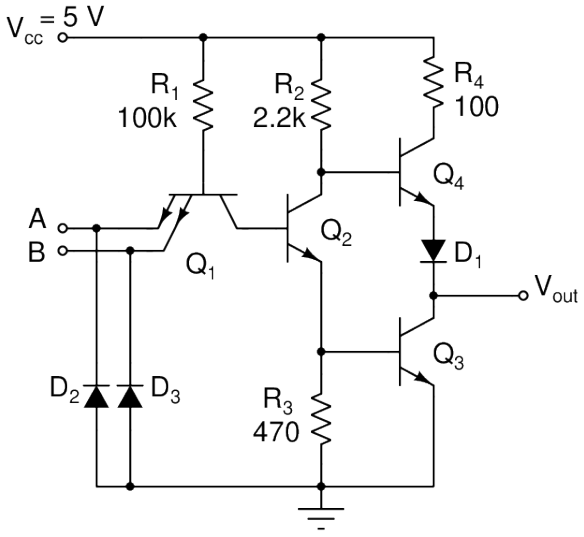


Fig. 4

(a) What is the function of diodes D_2 and D_3? [10%]

Solution:

They are *input clamp diodes* to protect the circuit when any of the inputs falls far below 0 V (e.g. ground bounce). D_2 or D_3 will be forward biased when that happens, and the voltages at A and B could not fall below -0.7 V.

(b) Explain the reverse/inverse active mode of a Bipolar (NPN) Junction Transistor (BJT). [10%]

Solution:

A bipolar transistor is in inverse active mode when the base-emitter junction is reversed-biased and the base-collector junction is forward-biased. The roles of emitter and collector interchange but the reverse gain β_R is much lower than the forward gain

β_F.

(c) Suppose both inputs A and B are high (5 V), show that the output voltage V_{out} will be close to 0.2 V. [20%]

Solution:

When both inputs are high, Q_1 is in *inverse active mode* and there will be a small current going into the base of Q_2, turning it ON.

The current is then drained through R_2 into the collector of Q_2, and from the emitter of Q_2, current flows through R_3 and the base of Q_3, turning it ON too.

Q_3 will be saturated and $V_{out} = V_{C3} = 0.2V$

(d) Suppose A is high (5 V) and B is low at 0.2 V, calculate the corresponding output voltage. [20%]

Solution:

When B is low, Q_1 is saturated: $V_{B1} = 0.2 + 0.7 = 0.9$ V, $V_{C1} = 0.2 + 0.2 = 0.4$ V.
Current is drained away from the base of Q_2 so Q_2 is turned OFF.

As a result, the base of Q_4 is pulled up to 5 V. Q_4 is then turned ON with $V_{BE4} = 0.7$.

The output voltage is therefore 5.0 - 0.7 - 0.7 (diode on-voltage drop) = 3.6 V.

(e) Explain why the maximum power dissipation of this design is around 8-10 mW. [20%]

Solution:

The current drawn from the power supply is higher when the output is low.

Similar to (b), we can deduce that $V_{B3} = 0.7$ V, $V_{B2} = 1.4$ V and $V_{B1} = 2.1$ V.

So,

$I_{B2} = (\frac{5 - 2.1}{100\text{k}})(2\beta_R + 1) = 34.8\ \mu$A and $I_{E2} = (\beta_F + 1)(34.8\mu) = 1.76$ mA

The power dissipation is approximately 5 V $\times$ 1.76 mA = 8.8 mW.

(cont.

(f) What is a Schottky transistor? Discuss how Schottky transistors can improve the performance of the TTL gate like the one in Fig. 4. [20%]

Solution:

Schottky transistor is a bipolar transistor with a Schottky barrier diode connected across the base-collector junction. The diode prevents the junction to become forward biased by more than 0.5 V so the transistor will not enter *deep saturation*.

Switching is faster when there is less charge accumulation in the base region of the transistor.

For example, by changing Q_1, Q_2 and Q_3 to Schottky transistor, it would take shorter time for them to switch from saturation (when output is low) to cut-off (when output is high) or vice-versa.

END OF PAPER

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