Version OBA/2

EGT2
ENGINEERING TRIPOS PART IIA

Friday 2 May 2025 09.30 to 11.10

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS

Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM

CUED approved calculator allowed

Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 (a) Use Shannon's expansion to find the canonical sum-of-products (SOP) form of the function $f = x_2 + \overline{x_1}\,\overline{x_3}$. [15%]

(b) Specify the size of a ROM that you could use to program the following two combinational circuits:

(i) An 8-bit adder/subtractor with C_{IN} and C_{OUT}. [5%]

(ii) An 8×8 multiplier. [5%]

(iii) Is using a ROM to implement the functions in part (b) (i) and (ii) a good design choice? Explain why or why not. [5%]

(c) A macro-cell, part of a complex combinational/sequential Programmable Array Logic (PAL) has been programmed as shown in Fig. 1. The binary gate signals on the *n*-channel MOSFET switches, G1 and G2, control the 2-1 multiplexers and the non-inverting tri-state buffers B1, B2, and B3. There are two main inputs labelled *X* and *Y* and one output labelled O1. The I/O2 pin can operate either as an extra input or the second output of the macro-cell. The bistable is of J-K type.

(i) Describe the multiple operations of the macro-cell and find the logic functions for all combinations of the gate signals G1 and G2. [30%]

(ii) Derive the state diagram if the macro-cell is operated as a state-machine. What type of architecture is the state-machine? [20%]

(iii) Consider that the macro-cell is operated as a state-machine and only output O1 is of interest. Draw a simplified block diagram of the circuit. What specific function does the circuit perform? [20%]

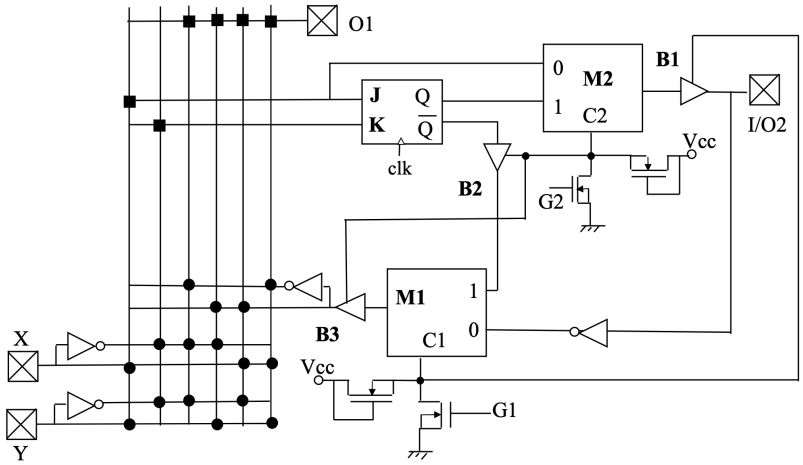

Fig. 1

2 (a) Compare and discuss EPROM, EEPROM and SRAM programming technologies. [20%]

(b) In order to automate its storage facilities, a warehouse has decided to design the sorting conveyor system shown in Fig. 2. The sorter controller can detect the length of incoming boxes (to be stored) and divert only the ones that are long. For simplicity, you may assume that all boxes are of only two sizes, either small or big. Using two sensors (S_1 and S_2), the small boxes will never pass under both sensors at one time, however, the big ones will. The sensor input will be set to logic high when a box is under the sensor; otherwise, it will remain at zero. After a big box is detected (i.e., the end of the box passes sensor S_2), the sorter must be activated, which will divert the box to the second output. You may also assume that there will always be sufficient space between boxes such that two boxes will never be under the sensors at the same time.

For all input sequences that are not physically possible, it needs to be ensured that the system returns to the initial state. Furthermore, all unused states should return the system to the initial state.

(i) Design the digital circuit for the sorter controller shown in Fig. 2. Draw the state diagram and the state table. [40%]

(ii) Draw the circuit implementation of the controller using J-K bistables and logic gates. [20%]

(iii) Comment on the existence of hazards, if any, in the implemented circuit. [20%]

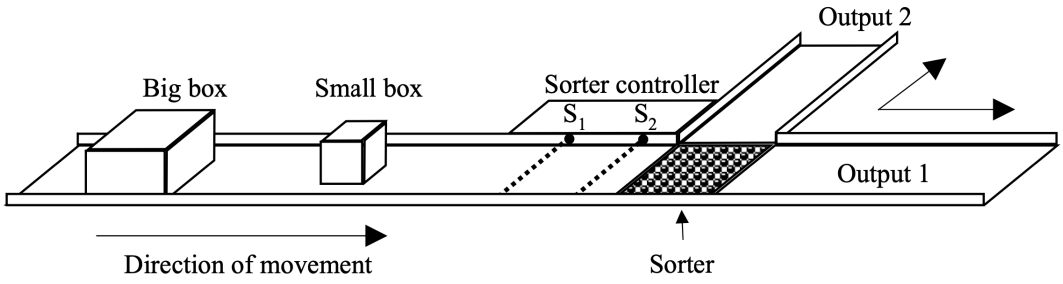

Fig. 2

3 (a) A microprocessor manufactured in 1996 operates at a rate of 10^6 calculations per second. Explain what rate of calculations you would expect from a microprocessor of the same price that has been manufactured four to five years later. [15%]

(b) NMOS inverters, which were popular before CMOS inverters, use a resistor to pull up the output. Explain briefly a drawback of NMOS inverters. [10%]

(c) A CMOS inverter is shown in Fig. 3. It is operated at a supply voltage of 2.5 V and is manufactured in a 0.25 μm process technology with the following parameters:

	NMOS	PMOS
Threshold voltage V_t (V)	0.43	−0.4
k' (μA/V^2)	115	−30

Assume that there is only capacitive load C_L at the output.

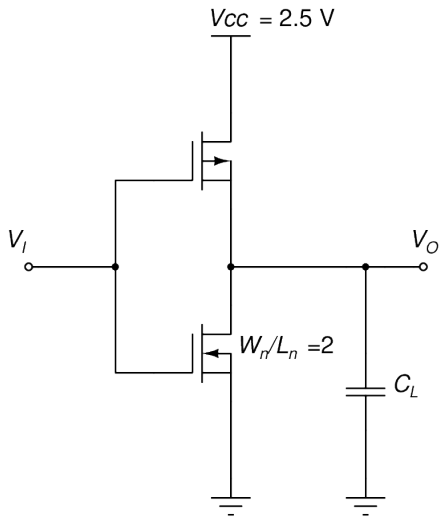

Fig. 3

(i) What would be the low output voltage V_{OL} of the inverter? Explain briefly the mode of operation of the NMOS transistor when V_O is close to V_{OL}. [15%]

(ii) Suppose a step input from 0 to 2.5 V is supplied to V_I at time $t = 0$. Sketch the change of V_O, which is initially 2.5 V, with respect to time. [10%]

(iii) What width-to-length ratio (W_p/L_p) for the PMOS transistor would make $V_I = V_O = 1.25$ V? You may make use of the fact that $|I_{Dp}| = |I_{Dn}|$. Ignore channel length modulation (i.e., $\lambda = 0$). [25%]

(cont.

(iv) If the switching speed of the inverter has to be further increased, what change(s) would you suggest and why? [15%]

The following current equations of a field-effect transistor may be useful:

$$k = k' \cdot \frac{W}{L}$$

$$I_D = k\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right) \qquad \text{for} \quad V_{DS} < V_{GS} - V_T$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \qquad \text{for} \quad V_{DS} \geq V_{GS} - V_T$$

(d) Suggest a new kind of transistor technology that could replace CMOS technology in the near future. State an advantage of this new kind of transistor technology. [10%]

4 A design of a transistor-transistor logic (TTL) 2-input NAND gate is shown in Fig. 4. The supply voltage V_{cc} is 5 V and all resistance values are provided in Ohm (Ω). Assume that the diode on-state voltage is 0.7 V, the transistor on-state base-emitter voltage and the saturated transistor collector-emitter voltage are 0.7 V and 0.2 V, respectively. The forward gain β_F is 50, and the reverse gain β_R is 0.1.

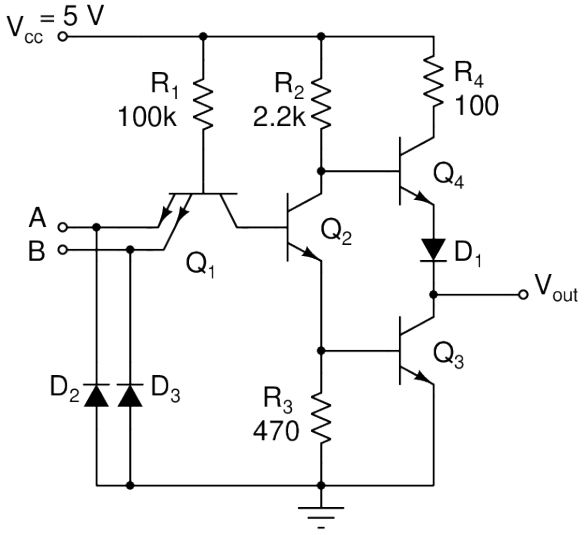

Fig. 4

(a) What is the function of diodes D_2 and D_3? [10%]

(b) Explain the reverse/inverse active mode of a Bipolar (NPN) Junction Transistor (BJT). [10%]

(c) Suppose both inputs A and B are high (5 V), show that the output voltage V_{out} will be close to 0.2 V. [20%]

(d) Suppose A is high (5 V) and B is low at 0.2 V, calculate the corresponding output voltage. [20%]

(e) Explain why the maximum power dissipation of this design is around 8-10 mW. [20%]

(f) What is a Schottky transistor? Discuss how Schottky transistors can improve the performance of the TTL gate like the one in Fig. 4. [20%]

END OF PAPER