1. (a) In digital circuits 'noise' means unwanted fluctuations of voltage or current superimposed on logic signals. Noise may be transferred to logic nodes or interconnecting wires through resistive, capacitive or inductive agencies.

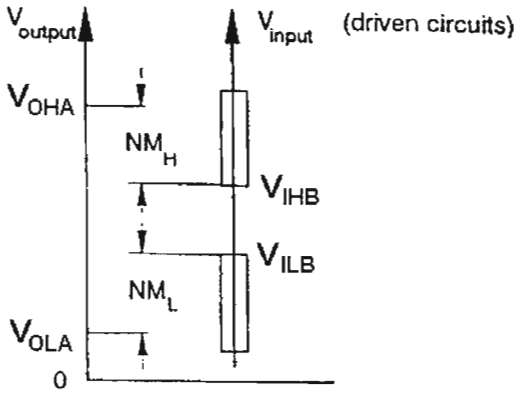
(i) Series resistance and/or inductance in ground or power lines that are shared by several logic elements may generate voltage drops with changing current and bring about injection of unwanted signals.

(ii) Capacitive coupling between wires or circuit tracks may result in unwanted coupling of a signal into an independent circuit. Inductive coupling (mutual inductance) may result in changing currents generating induced voltages in neighbouring wires.

(iii) Direct radiation of RF signals from outside sources into poorly screened wires within the system can generate spurious voltages and currents.

Any of these effects is likely to cause time-varying fluctuations or 'noise', independent of the desired signals.

If the magnitude of noise is too great at any point of the circuit, it is liable to cause errors of logic. Correspondingly, if the noise amplitude is smaller than a certain critical magnitude, known as the *noise margin* of that circuit, the noise component will be attenuated as the signal passes from input to output of the corresponding logic gate, and will not propagate further. As a properly functioning logic circuit is required not to exhibit errors of logic, this is an important principle, and a logic designer must be aware of the levels of noise originating inside or outside the system and choose combinations of logic families so that the noise margins are not exceeded.



V_{OHA} and V_{OLA} represent respectively:

- the lowest voltage supplied by logic circuit A delivering logic '1', and
- the highest voltage supplied by an output delivering logic '0'

V_{IHB} and V_{ILB} represent respectively:

- the lowest input to B acceptable as logic '1'
- the highest input to B acceptable as logic '0'

If the output of A is connected to the input of B, the noise margins observed in the High and Low states are:

$$NM_H = V_{OHA} - V_{IHB} \qquad \text{and} \qquad NM_L = V_{ILB} - V_{OLA}$$

Both noise margins must be positive if the pair of circuits is to operate consistently. Their magnitude must be δ or greater if superimposed noise of voltage magnitude up to δ is to be rejected.

Note that the voltages V_{OH} and V_{OL} are liable to depend on the magnitude of the current flowing in the corresponding output devices – i.e. they depend on fan-out.

	V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{IHmax}	I_{ILmax}
CMOS	**1.0 V**	**3.5 V**	**0.1 V**	**4.9 V**	**0**	**0**
ALS-TTL	**0.8 V**	**2.0 V**	**0.5 V**	**2.5 V**	**20 μA**	**-100 μA**

(i) CMOS drives ALS-TTL

$N_{MH} = V_{OHcmos} - V_{IHals\text{-}ttl} = 4.9 - 2.0 = 2.9$ V

$N_{ML} = V_{ILals\text{-}ttl} - V_{OLcmos} = 0.8 - 0.1 = 0.7$ V

(ii) ALS-TTL drives CMOS

$N_{MH} = V_{OHals\text{-}ttl} - V_{IHcmos} = 2.5 - 3.5 = -1.0$ V

$N_{ML} = V_{ILcmos} - V_{OLals\text{-}ttl} = 1.0 - 0.5 = 0.5$ V

(i) will work satisfactorily but note that it will be significantly more susceptible to noise in the low state.

(ii) would not work since $N_{MH} < 0$

If operated with fanout of 30 (i.e. 30 inputs were driven), the ALS-TTL → CMOS margins (for operation assumed to be static or low-frequency) would be unaffected, since the table indicates that CMOS gates draw no input current.

The CMOS → ALS-TTL noise margins are liable to be affected by the large fanout.

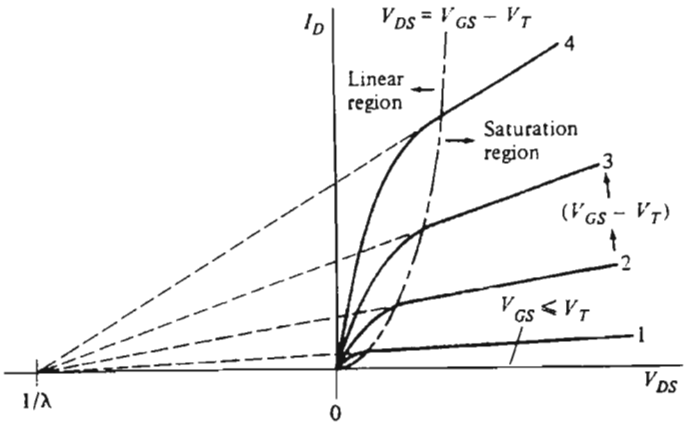
With the CMOS output high, the CMOS gate must source $30 \times 20 = 600$ μA when delivering '1' to the following 30 ALS-TTL gates. This is not a particularly onerous demand.

With the CMOS output low, the CMOS gate must sink a total of $30 \times 0.1 = 3$ mA at its output, from the following ALS-TTL inputs. This might be beyond its capacity, or if not, it is liable to raise V_{OLcmos} and erode still further the already poor noise margin in the low state.

In either case, with 30 inputs driven, the additional capacitance will affect the rise/fall time achieved. Full analysis calls for more information about the devices in use and their dimensions, which determine the ability of the output stages to source/sink current to charge/discharge this parasitic load, but drivers implemented in CMOS are often limited cf some bipolar families in terms of available output current.

2 (a) There are several reasons: (i) The resistors take too large area to be implemented in silicon technology compared to transistors (ii)The digital margins are lower in case of a resistor being used as the lead element (iii) The power consumption during steady state is very high in case of using resistors. This is because the load is a p-channel device while the driver is an n-channel. The mobility of holes is reduced compared to that of electrons (by a factor of 3). This is why the perimeter (or W/L) of the p-channel transistors is made 3 times larger.

2.
(b)



Eq 1
Linear region

Eq 2
Saturation region

←Increasing V_{GS} (1-4)

n-channel enhancement mode MOSFET

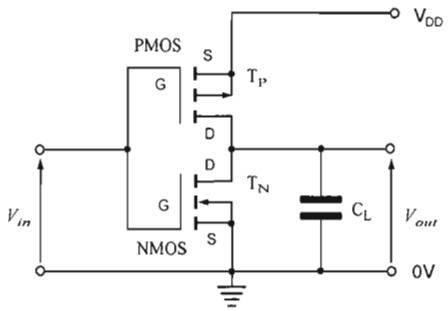
Vertical scale exaggerated to emphasise channel-length modulation effect

(c) Equation 2 predicts that I_D is independent of V_{DS}. The observed behaviour is a gradual increase in I_D with V_{DS}, owing to shortening of the channel – the gradual extension of the pinch off region as V_{DS} rises beyond $V_{GS}-V_T$. This can be modelled as follows:

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \qquad 2'$$

λ is referred to as the *channel length modulation coefficient* and is typically 0.01 – 0.1 V^{-1}. The same $(1+\lambda V_{DS})$ factor may be applied to Equation 1 to ensure continuity at the point $V_{DS} = V_{GS} - V_T$. Another factor affecting I_D is the body effect, in which the potential of the source electrode relative to the substrate affects the channel conductance.

(d) The circuit for the complementary MOS inverter is shown.



Note that since both devices have the same k and $|V_T|$, delays and rise/fall times are the same for both transitions, 0-1 and 1-0.

We shall assume that (i) equations 1 and 2 can be used as given, (ii) that the input changes abruptly, and (iii) there is no load apart from the 10 pF capacitance; (iv) V_{OH} and V_{OL} for the inverter are V_{DD} and 0 V.

The delay time is asked for the output making its transition from 1 to 0. This is caused by the input switching from 0 to 1 at $t = 0$; the abrupt transition means that T_P switches off instantly, and we need only consider the discharge of C_L thru T_N. We now consider the changing conditions for this device. At the instant T_N begins to conduct, V_{out} is V_{DD}, V_{GS}= V_{DD} and V_{DS} is also V_{DD}. Noting this is a n-channel device, we see it is clearly in its saturation region, in which it will remain until V_{DS} falls to $V_{GS} - |V_T|$, or (in this case) until V_{out} falls to 2 V. The remainder of the fall happens with T_N in its non-saturation/linear region.

We are interested in the time that elapses before V_{out} falls to the value corresponding to 50% of the logic swing, which we shall assume to extend from V_{DD} to 0 V. Hence (in this case) we want the interval between $t = 0$ and the instant at which V_{out} passes through 1.5 V. This interval comprises two periods that have to be found:

t_{SAT} - C_L discharges from 3.0 V to 2.0 V (T_N in saturation region – Eqn 2)
$t_{NON\text{-}SAT}$ - C_L discharges from 2.0 V to 1.5 V (T_N in non-sat'n region – Eqn 1).

For t_{SAT}, T_N in its saturation region acts as a constant current source with current:

$$I_D = \frac{k}{2}(V_{GS} - |V_T|)^2 = \frac{k}{2}(3-1)^2 = 2k$$

The time t_{SAT} taken to discharge C_L through 1.0 V at constant current is:

$$t_{SAT} = C_L \times |V_T| / I_D = 1.0 \times C_L / 2k = 0.5\frac{C_L}{k}$$

As V_{out} reaches 2 V, T_N enters its non-saturation region and the current thereafter depends on its V_{DS} and hence on V_{out}. The general expression for I_D (NMOS case) is then:

$$I_D = \frac{k}{2}\left[2(V_{GS} - |V_T|)V_{DS} - V_{DS}^2\right] \qquad \text{(i)}$$

Using the same approach as before we can write:

$\frac{dV_{out}}{dt} = -\frac{I_D}{C_L}$ and noting that $V_{DS} = V_{out}$, we have from (i):

$$t_{NON-SAT} = \int_0^{t_{NON-SAT}} dt = -C_L \int_{V_1}^{V_2} \frac{1}{I_D} dV_{out} = -C_L \int_{V_1}^{V_2} \frac{dV_{out}}{\frac{k}{2}\left[2(V_{GS} - V_T)V_{out} - V_{out}^2\right]}$$

The total rise time is the sum of the intervals in the saturation and non-saturation regions.

Hence a general expression is: $\underline{t_{delay} = t_{SAT} + t_{NON-SAT}}$, (ii)

with t_{SAT} and $t_{NON\text{-}SAT}$ determined as above. Substituting into the two general expressions:

$$t_{SAT} = 1.0 \times C_L / 2k = \frac{C_L}{2k}$$

for the saturation part of the interval. For the non-saturation part,

$$I_D = \frac{k}{2}\left[2(3-1)V_{out} - V_{out}{}^2\right] = \frac{k}{2}\left(4V_{out} - V_{out}^2\right) = \frac{k}{2}(V_{out})(4 - V_{out})$$

and substituting this into the general expression for $t_{NON\text{-}SAT}$ we get:

$$\int_0^{t_{NON-SAT}} dt = t_{NON-SAT} = -\frac{2C_L}{k}\int_2^{1.5} \frac{dV_{out}}{V_{out}(4 - V_{out})}$$

This can be simplified using partial fractions to: $-\frac{2C_L}{k}\int_2^{1.5} \frac{1}{4}\left(\frac{1}{V_{out}} + \frac{1}{4 - V_{out}}\right)dV_{out}$

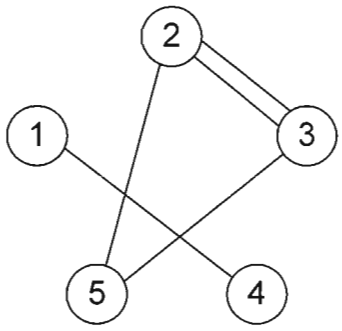
Hence

$$t_{NON-SAT} = -\frac{C_L}{2k}\left[\ln\left(V_{out} \times (4 - V_{out})\right)\right]_2^{1.5} = -\frac{C_L}{2k}\left(\ln(2.5 \times 1.5) - \ln(2 \times 2)\right) = -\frac{C_L}{2k}\ln\left(\frac{3.75}{4}\right)$$

Using (ii), $t_{delay} = \frac{10 \times 10^{-12}}{2 \times 10 \times 10^{-6}} \times (1 + (-\ln 0.94)) = 0.5 \times 10^{-6} \times 1.06 = \underline{0.53\ \mu S}$

To reduce the switching time, reduce C or consider increasing V_{DD}: but note that this will increase power consumption. Magnifying k by increasing W/L is also worth considering, as it may deliver an improvement, but note that this will also increase the contribution to parasitic capacitance made by T_N and T_P. The effectiveness of this approach will depend on how C_L is distributed between the drains of the FETs, the wiring, and the driven capacitances, and we are not told this.

3. (a) Only one merging can be done (2 &3) with identical outputs. This reduces the state table to 4 states.



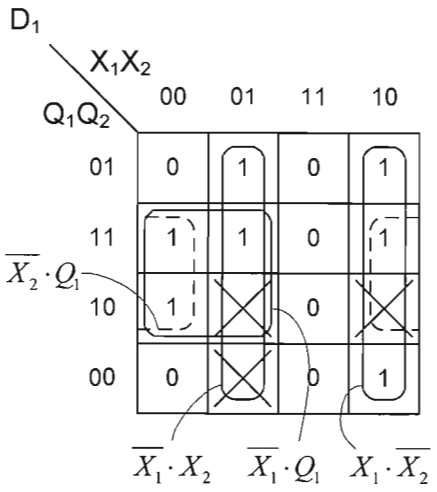
Present State	Next state for X_1X_2 = 00	01	11	10	Z_1Z_2
①	①	2	4	3	01
②③	5	②	4	③	11
④	1	--	④	3	00
⑤	5	--	4	--	10

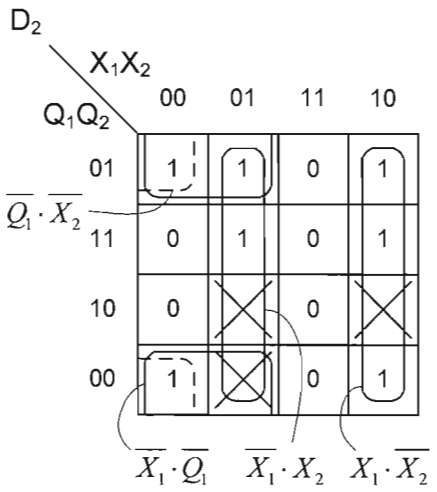
Present State $Q_1Q_2 \equiv Z_1Z_2$	Next state for X_1X_2 = 00	01	11	10	Input D_1 for bistable whose output is Z_1, X_1X_2 = 00	01	11	10	Input D_2 for X_1X_2 = 00	01	11	10
① 01	01	11	00	11	0	1	0	1	1	1	0	1
②③ 11	10	11	00	11	1	1	0	1	0	1	0	1
④ 00	01	--	00	11	0	--	0	1	1	--	0	1
⑤ 10	10	--	00	--	1	--	0	--	0	--	0	--

A B

[25%]

The bistable inputs D1 and D2 are the next states. The outputs are the same as Q1 and Q2. The k-maps are shown below:





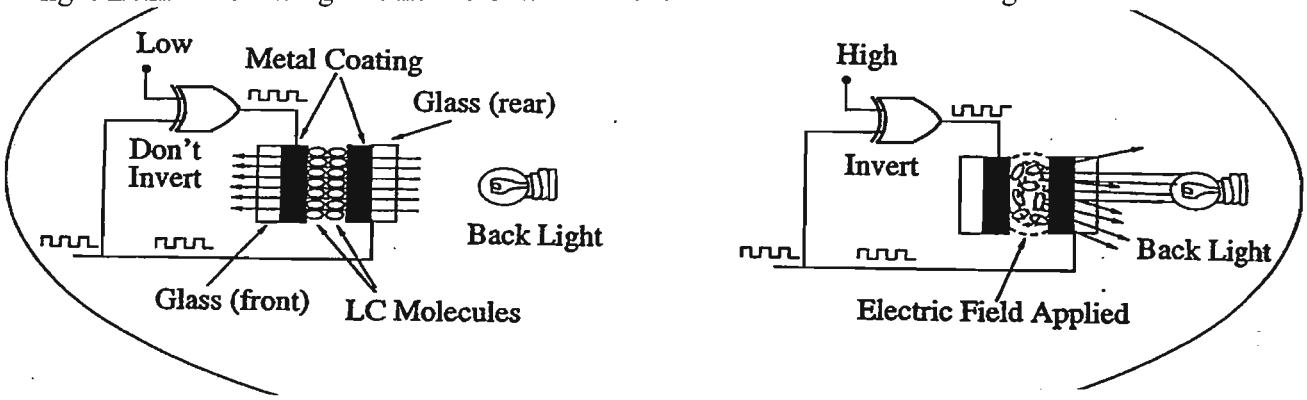
So $D_1 = \overline{X_1} \cdot X_2 + X_1 \cdot \overline{X_2} + \overline{X_1} \cdot Q_1 + Q_1 \cdot \overline{X_2}$ *

$D_2 = \overline{X_1} \cdot X_2 + X_1 \cdot \overline{X_2} + \overline{X_1} \cdot \overline{Q_1} + \overline{Q_1} \cdot \overline{X_2}$ *

* Added terms to make logic hazard free

[25%]

(b) (i) The 8-bit converter takes the signal from the potential divider (with the thermistor on the low side) and converts it into a digital block. The PROM adapts the signal from the 8 bit ADC to a form that is suitable to be input to the two blocks of BCD to LCD seven segment displays. The 30 Hz is connected to the back plane of the inverters and through a XOR gate to the output signals of each of the segment outputs from the LCD decoders. When two signals are in phase and there is no electric field between the back plane and front plane, the light coming from the back light is allowed through - this is the case of a 'lit' segment. When two signals are out of phase and an electric field is created between the back plane and front plane, which results in the molecules being disorganised and the light from the back-light is now blocked – this is a the case of the 'dark segment'.



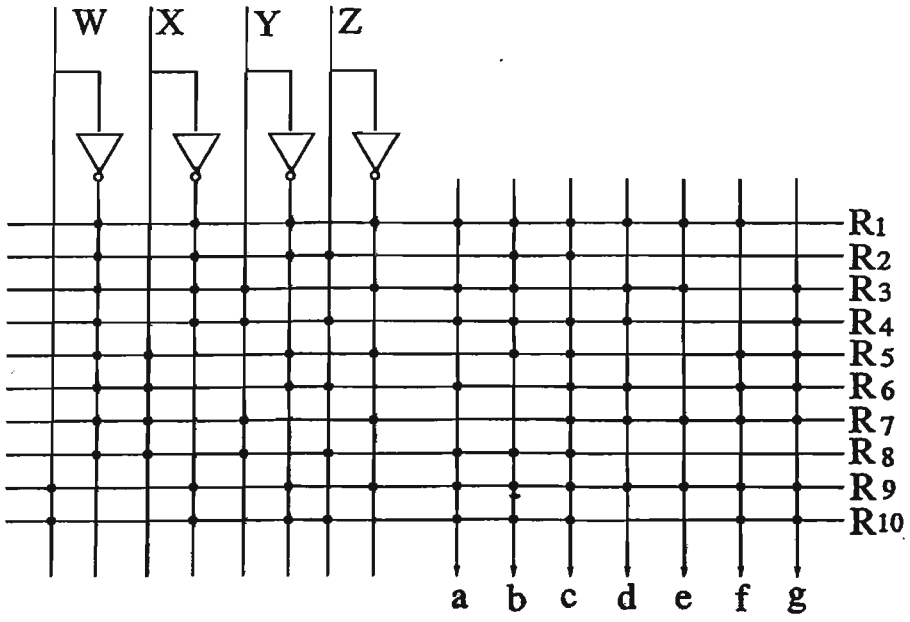
[15%]

(ii) The size of the EPROM is 2^8x8 bits = 256 x8 bits.

Given the 8 bit ADC, there are 2^8-1=255 quantization levels. The maximum analogue signal present at the output of the potential divider is 5V and the minimum 0V. The ADC voltage resolution is 5-0/255= 19.6mV

[15%]

(iii) asuming that the LCD decoder also contains the controlled XOR inverters, the PLA implementation is shown below. The outputs a,b,c,d,e,f, g are then connected to a network of XOR gates as shown above.

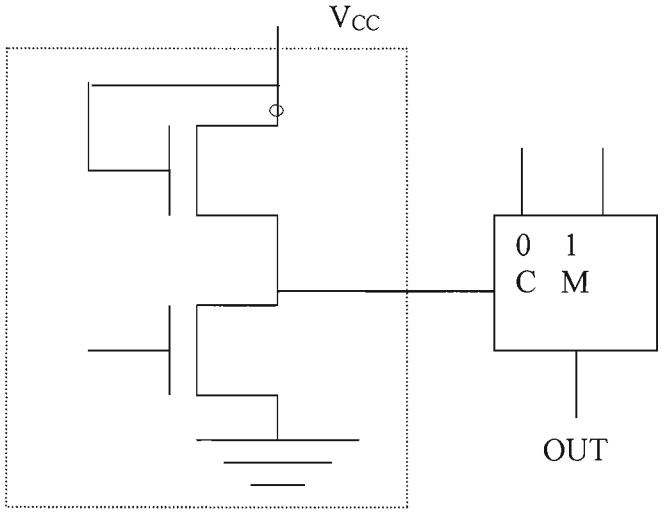


[20%]

4(a) The PROM (memory array programmable and AND array fixed) are the most common and they are the least expensive. They are suited for multiple combinational functions with relatively few variables. The PLAs (both AND and OR arrays are programmable) are the most flexible and can allow implementation of multiple functions with a high number of variables. The PALs (AND array programmable and OR array fixed) are less powerful than PLAs but significantly cheaper. [20%]

b) The control circuits connected to M_1 and M_2 are NMOS inverters.

$G = 0 \Rightarrow C = 1$
$G = 1 \Rightarrow C = 0$



NMOS INVERTER

- If $G_1 = 1 \Rightarrow C_1 = 0 \Rightarrow I/O_2$ is configured as input, $I/O_2 = I$. The input I is selected at the M_1 multiplexer and becomes (or not) an input in the PAL function of G2.

In this case the macro-cell behaves as a single output combinational circuit with 3 inputs X, Y, I. However O1 does not depend on I and therefore is only a function of X and Y. The logic function implemented is:

$$O_1 = \overline{X} + \overline{Y}$$

- If $G_1 = 0$ and $G_2 = 1 \Rightarrow C_1 = 1, C_2 = 0$

B_2 and B_3 are inactive and $I/O_2 = O_2$.

The bistable is bypassed and the macro-cell behaves as a two output combinational network with two inputs.

$$\begin{cases} O_1 = \overline{X} + \overline{Y} \\ O_2 = XY \end{cases}$$

- If $G_1 = 0$ and $G_2 = 0 \Rightarrow C_1 = 1, C_2 = 1$

B_1, B_2 and B_3 are shortcircuits, M_1 and M_2 select the input "1". The cell behaves as a MEALY sequential circuit with two outputs O_1 and O_2. Using reverse method we can work out Q^+ and T.

$$\left.\begin{array}{l} Q^+ = Q \text{ if } T = 0 \\ Q^+ = \overline{Q} \text{ if } T = 1 \end{array}\right\} \Rightarrow Q^+ = Q\overline{T} + \overline{Q}T$$

$$\begin{cases} T = \overline{Q}XY \\ Q^+ = Q\overline{T} + \overline{Q}T = Q(Q + \overline{XY}) + \overline{Q}XY = Q + \overline{Q}XY = Q + XY \end{cases}$$

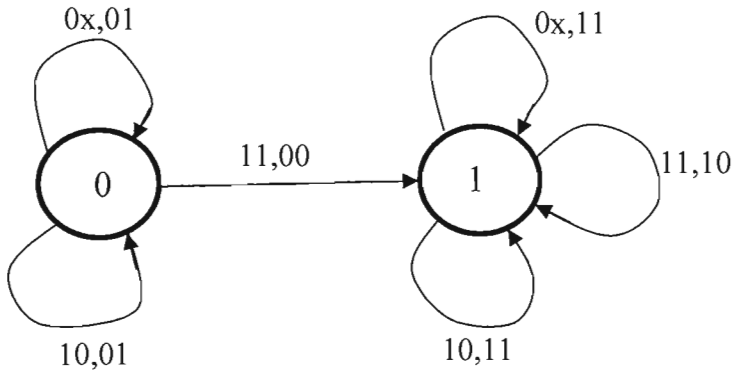
$O_1 = \overline{X} + \overline{Y}$

$O_2 = Q$

[40%]

State table & state diagram.

Q	Q^+ for Input XY =				O_2O_1 output for XY =			
	00	01	11	10	00	01	11	10
0	0	0	1	0	01	01	00	01
1	1	1	1	1	11	11	10	11



[40%]