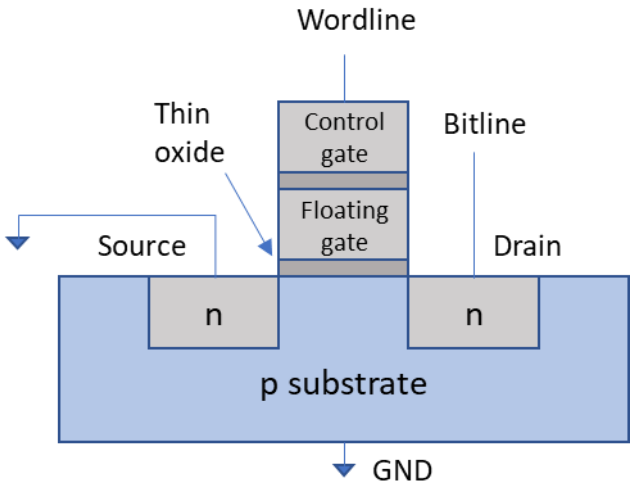
1 (a) Flash memory is a nonvolatile memory because it retains its contents after power is turned off. Flash memory allows the user to electrically program and erase information. Flash memory uses memory cells similar to an EEPROM, but with a much thinner, precisely grown oxide between a floating gate and the substrate (see figure below).



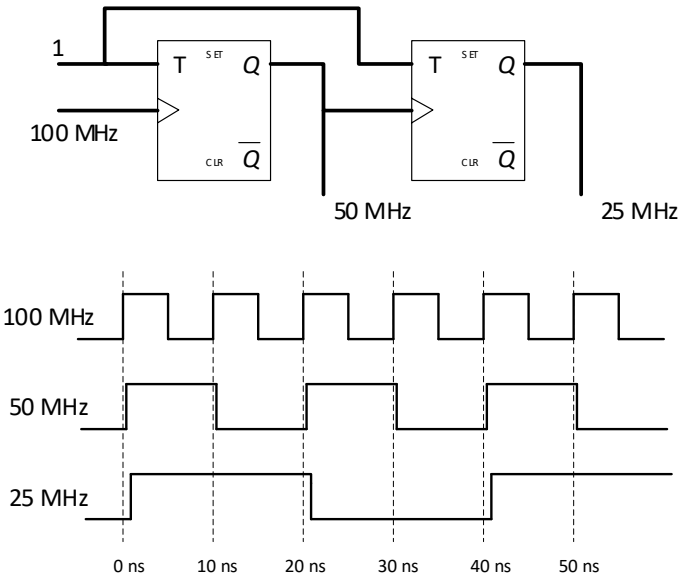
Flash programming occurs when electrons are placed on the floating gate. This is done by forcing a large voltage (usually 10 to 12 volts) on the control gate. Electrons quantum-mechanically tunnel from the source through the thin oxide onto the control gate. Because the floating gate is completely insulated by oxide, the charges are trapped on the floating gate during normal operation. If electrons are stored on the floating gate, it blocks the effect of the control gate. The electrons on the floating gate can be removed by reversing the procedure, i.e., by placing a large negative voltage on the control gate. The default state of a flash bitcell (when there are no electrons on the floating gate) is ON, because the channel will conduct when the wordline is HIGH. After the bitcell is programmed (i.e., when there are electrons on the floating gate), the state of the bitcell is OFF, because the floating gate blocks the effect of the control gate. Flash memory is a key element in thumb drives, cell phones, digital cameras, and other low-power devices that must retain their memory when turned off.

[20%]

(b) The code in Figure 1 represents a multiplier. It multiplies the lower two bits of Input by the upper two bits of Input, producing the four-bit Output. The style of code is poor, because it is not readily apparent what is being described.

[20%]

(c)



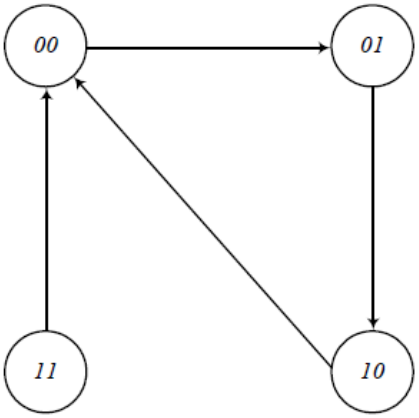
[20%]

(d) (i) Using the bistable transition table we can create the table below:

Present state		Input		Next state	
A	B	TA	TB	A+	B+
0	0	0	1	0	1
0	1	1	1	1	0
1	0	1	0	0	0
1	1	1	1	0	0

[10%]

(ii) A state diagram can be sketched from (i):



[10%]

(iii) A counter with a repeated sequence of 00, 01, 10. Counters are some of the most used circuits in digital electronics. Plenty of examples given during the course. [20%]

Assessor's comments: A popular question. Very few described the floating gate role in programming a bit, while some attempted to use counters in part (c), although bistables were required. Parts (b) and (d) were reasonably answered.

2 (a) FSMs (i.e. state diagrams and tables) are convenient for describing the behavior of circuits that have only a few inputs and outputs. For larger circuits (machines) we often need (use) ASM charts, which are similar to traditional flowcharts. However, unlike traditional flowcharts, they include timing information because it implicitly specifies that the FSM changes (flows) from one state to another only after each active clock edge. The ASM charts can be used to describe complex circuits that include one or more FSMs and other circuitry such as registers, shift registers, counters, adders, and multipliers.

[20%]

(b) Expansion in terms of x_1 gives:

$$f = \overline{x_1}x_2 + \overline{x_1 x_3} + x_1 x_2$$

Further expansion in terms of x_2 gives:

$$\begin{aligned} f &= \overline{x_2}\,(\overline{x_1 x_3}) + x_2(x_1 + \overline{x_1} + \overline{x_1 x_3}) \\ &= \overline{x_1}x_2 + \overline{x_1}x_2\overline{x_3} + \overline{x_1 x_2 x_3} + x_1 x_2 \end{aligned}$$

Further expansion in terms of x_3 gives:

$$\begin{aligned} f &= \overline{x_3}\,(\overline{x_1 x_2} + x_1 x_2 + \overline{x_1}x_2 + \overline{x_1}x_2) + x_3(x_1 x_2 + \overline{x_1}x_2) \\ &= \overline{x_1 x_2 x_3} + x_1 x_2\overline{x_3} + \overline{x_1}x_2\overline{x_3} + \overline{x_1}x_2 x_3 + x_1 x_2 x_3 \end{aligned}$$

[30%]

(c) (i) Y = F(A,B,C,D,E,F,G,H,I) = ABCDEFGHI

[10%]

(ii) Y = F(A,B,C,D,E,F,G,H) = ABCD + ABCDE + FGH

[10%]

(d) (i) Number of inputs = 2 × 16 + 1 = 33

Number of outputs = 16 + 1 = 17

Thus, this would require a 2^{33} x 17-bit ROM.

[10%]

(ii) Number of inputs = 16

Number of outputs = 16

Thus, this would require a 2^{16} x 16-bit ROM. [10%]

(iii) These implementations are not good design choices. They could be implemented in a smaller amount of hardware using discrete gates. [10%]

Assessor's comments: Very few used Shannon's expansion in part (b), although this was clearly required, while many got confused with the general size of a ROM in part (d). Parts (a) and (c) were well answered, although in part (a) very few made a complete discussion.

3 (a) Due to approaching the limits of miniaturing and due to the heat dissipation problem, among others, it is harder to develop much faster processors. Therefore, to increase the computational power, the computational load is distributed to several cores. [15%]

(b) (i) It is obvious that the around C=1M, the logic gate enters the high gain region and around C=2M, the logic gate exits this region. Hence, C_{IL}=1M and C_{IH}=2M. For C_{IL}, answers larger than 0.5M and for C_{IH}, answers smaller than 2.5M can be accepted. [10%]

(ii) Similarly, V_{OL}=1.7V and V_{OH}=4.2V. This part depends on the answer to the previous part as well. [10%]

(iii) Logic swing depends on the answer to part (ii) but it is approximately 2.5V. [5%]

(c) (i) D_1 prevents the coupling between Q_4 and Q_3 when the output is low. When the output is low, $F = V_{CE(sat)}$ and $V_{2E} = V_{BE(on)}$, due to Q_3 being in saturation. Since Q_2 is also in saturation, $V_{2C} = V_{4B} = V_{CE(sat)} + V_{BE(on)}$. Hence, $V_{4BE} = V_{BE(on)}$. This means that Q_4 might turn on when it is supposed to be off, causing unstable operation. D_1 increases the necessary V_{4B} for it to be activated. [15%]

(ii) D_1 could also be situated on the base of Q_4. Similar to the previous case, Q_{2C} will not be enough to activate Q_4. [15%]

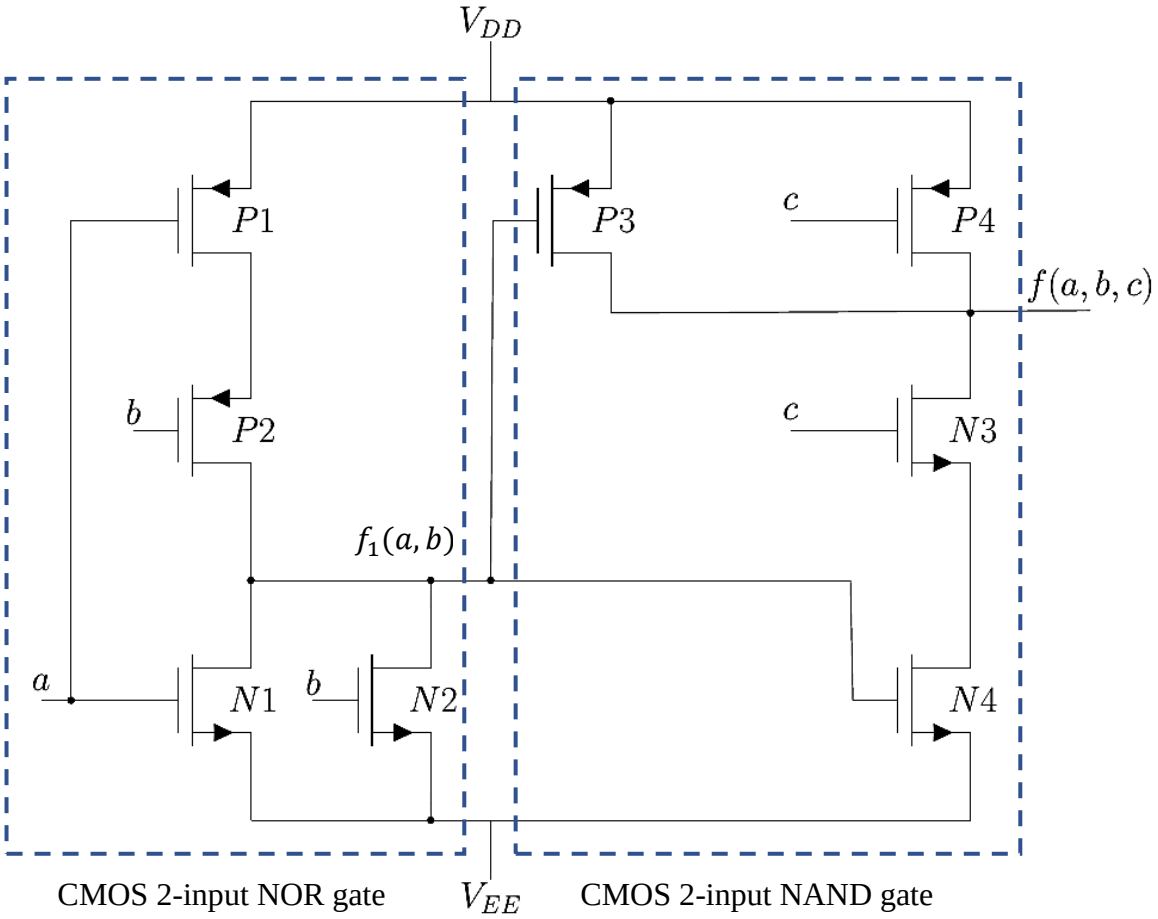
(iii) Diodes have very low forward resistances. Therefore, D_1 dissipates minimum amount of energy. A resistor would also increase the necessary V_{4B} for Q_4 to be activated, but at the cost of increased energy consumption. The voltage drop across the diode is constant while voltage drop across the resistor depends on the current. Hence, when the output is high, if D_1 is replaced by a resistor, the fanout will be lower. [15%]

(iv) Changing R_3 causes a delay-power tradeoff. Higher R_3 reduces the base current for Q_4 and increases the time it takes for C_{4BE}. Hence, increased R_3 increases t_{LH}, as Q_4 gets activated during the low-to-high transition. Lower R_3 on the other hand, increases the power dissipation. When the output is low, $V_{2C} = V_{CE(sat)} + V_{BE(on)}$. Then, we can find the potential across R_3 as $V_{R3} = V_{CC} - V_{BE(on)} - V_{CE(sat)}$. Since the potential on R_3 is constant, lower resistance implies higher power dissipation. [15%]

Assessor's Comments:
This was a popular question with 52 attempts out of a total of 70 students. The mean was 46.9 out of 100 with a standard deviation of 17.3. The aim of part (a) was to make students use their newly obtained knowledge to explain recent trends in the emergence of multi-core microprocessors in the last decade. A large group of students were confused about the causes and outcomes of this development. Part (b) focused on transferring basic concepts from transistors to bioFETs in digital design. Large portion of the attempts here received either full or close to full marks. Since part (b)(ii) depended on the answer given in part (b)(i) and part (b)(iii) depended on the answer given in part (b)(ii), errors carried forward from earlier stages still received full marks. Part (c) was about a TTL circuitry

discussed in the lectures. The answers showed surprising diversity, but overall, students showed that they grasped all basic concepts regarding TTL.

4 (a) The circuit contains a CMOS 2-input NOR gate and a CMOS 2-input NAND gate as shown below:



Thus, $f_1(a,b) = \overline{a+b}$ and $f(a,b,c) = \overline{f_1(a,b).c} = \overline{(\overline{a+b}).c}$, which can be simplified as $f(a,b,c) = a + b + \bar{c}$. [40%]

(b) The transistors P2, N1 and N3 are in cut-off due to the applied input voltages. For N2, $i_D = 0$, thus, V_{DS}= 0V. Thus, 0 V is applied to the gate of N4 and this transistor is also in cut-off. In addition, 0 V is applied to the gate of both P3 and P4 transistors. Depending on output voltage, P3 and P4 can be either in saturation or linear region.

If P3 and P4 are in saturation region, their drain current is derived based on $I_D = \frac{1}{2}k\,(V_{SG} - |V_T|)^2$. The output current passing through R_L is then $I_L = 2\,I_D = 2 \times \frac{1}{2} \times 1 \times (5-1)^2 = 16\,mA$. This leads to $V_{output} = 16\,V$, thus, $V_{SD} = -11\,V$ for both P3 and P4 transistors. Thus, the transistors cannot be in saturation mode.

If P3 and P4 are in linear mode, their drain current is derived as $I_D = k[(V_{SG} - |V_T|)\,V_{SD} - 0.5\,V_{SD}^2]$. The drain voltage of these transistors is equal to the output voltage, thus, $V_D = 2R_L I_D = 2R_L k[(V_{SG} - |V_T|)\,V_{SD} - 0.5\,V_{SD}^2]$. This leads to $V_D = \frac{1+\sqrt{61}}{2}$= 4.4 V and $I_L = 4.4\,mA$. [40%]

(c) The circuit contains two layers of calculation. When a or b are changed, they will first affect the value of $f1(a,b)$. Then, $f1(a,b)$ and c are used to find $f(a,b,c)$. Thus, changing a or b takes longer to affect the output compared to changes in c. [20%]

Assessor's Comments:

This was one of the popular questions of the exam, with 63 students out of 70 attempted. The average was 70.6 out of 100 with a standard deviation of 23.8. The aim of the question was to evaluate the students' understanding of transistors' working principle, their use in building logic circuits and the signal propagation delay in electronic circuits. Students performance was better in part (a) of the question, which focused on deriving the implemented function by a circuit. While some students did not recognize the sub-parts of the circuit, i.e., CMOS 2-input NOR and NAND gates, they were still able to solve this part by finding the output for different combinations of inputs, which is a bit time consuming. Students had more calculation errors in part (b), where they needed to identify which transistors are in cut off and which are active due to the applied bias. Part (c) was observed more straightforwardly by the students as they only needed to realise the inputs that pass through more layers of calculation but some students have confused it with the delay of PMOS vs NMOS.