Version FU/6

EGT2
ENGINEERING TRIPOS PART IIA

Monday 5 May 2014 9.30 to 11

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) Explain what is meant by the term *noise margin* when applied to an assembly of logic gates. With the aid of a diagram, show how to determine the noise margins for a pair of connected logic gates from the characteristic input and output levels V_{IL}, V_{IH}, V_{OL} and V_{OH}. [30%]

(b) Why is it important when interconnecting logic gates from different families to pay careful attention to the noise margins that apply? Discuss briefly electronic phenomena encountered in practical situations that may cause incorrect operation if noise margins are not appropriately defined. [30%]

(c) Characteristic input and output voltages for inverter gates taken from a manufacturer's 5 volt *Advanced Low-power Schottky TTL* (ALS-TTL) and CMOS logic catalogue are given in the table below, which also show the maximum input currents flowing into the device in the high and low logic states.

	V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{IHmax}	I_{ILmax}
CMOS	**1.0 V**	**3.5 V**	**0.1 V**	**4.9 V**	**0**	**0**
ALS-TTL	**0.8 V**	**2.0 V**	**0.5 V**	**2.5 V**	**20 μA**	**-100 μA**

Determine the noise margins that will apply when:

(i) a CMOS inverter drives a single ALS-TTL inverter input; [10%]

(ii) an ALS-TTL inverter drives a single CMOS inverter input. [10%]

Comment on these results. How would you expect the noise margins to be affected in each case if thirty inputs were driven instead of one? State any assumptions made. [20%]

2 (a) Why is it better to use transistors rather than resistors as the load element in MOSFET inverters? Explain carefully why it is customary in CMOS logic gates for the load and driver devices to have different dimensions. [20%]

(b) The drain current I_D for a MOSFET may be modelled either by equation (1) or by equation (2) according to the region in which the device is operating. Sketch a typical output characteristic for a MOSFET and show clearly on your graph the regions in which the two equations may be applied. Name the regions. [20%]

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad V_{DS} < (V_{GS} - V_T) \qquad (1)$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \qquad V_{DS} \geq (V_{GS} - V_T) \qquad (2)$$

Discuss the limitations of equation (2) for describing the behaviour of the device in the applicable region, and suggest how the equation can be modified to model more accurately the observed dependencies. [10%]

(c) A complementary MOS inverter is fabricated from two transistors each of device transconductance k, and is run from a 3 V supply. The threshold voltages of the NMOS and PMOS devices are 1 V and –1 V respectively. The output terminal is connected to a purely capacitive load C_L.

Derive an expression for the delay imposed on a signal propagated through the inverter, assuming that the input voltage changes abruptly from logic 1 to logic 0. State any other assumptions made. If k = 10 μA V^{-2} and the external load C_L is 10 pF, calculate the actual delay. Discuss briefly how the switching speed might be improved. [50%]

3. (a) A reduced state table for a system for which merging is to be performed is shown in Fig. 2.

(i) Draw a Merger diagram and show a reduced state table suitable for a Moore architecture. [25%]

(ii) If the bistable allocation for the states is to be identical to the two bit output Z_1Z_2, using D-type bistables, find what the inputs D_1 and D_2 should be for the two bistables. [25%]

(b) Fig. 3 shows a schematic diagram of a digital Celsius thermometer. The thermistor is a highly sensitive, non-linear temperature sensor. The PROM is used to convert the signal from the *Analogue to Digital Converter* (ADC) into the two 4-bit BCD strings. The displays are made of seven segment *Liquid Crystal Displays* (LCDs).

(i) Describe briefly the operation of the various blocks highlighting the need for the 30 Hz backplane oscillator. [15%]

(ii) Determine the size of the PROM memory and the ADC voltage resolution. [15%]

(iii) Show the implementation of one of the LCD decoders using a PLA. [20%]

X_1X_2 00	01	11	10	Z_1Z_2
(1)	2	4	3	01
5	(2)	--	3	11
5	2	4	(3)	11
1	--	(4)	3	00
(5)	--	4	--	10

Fig. 2

(cont.

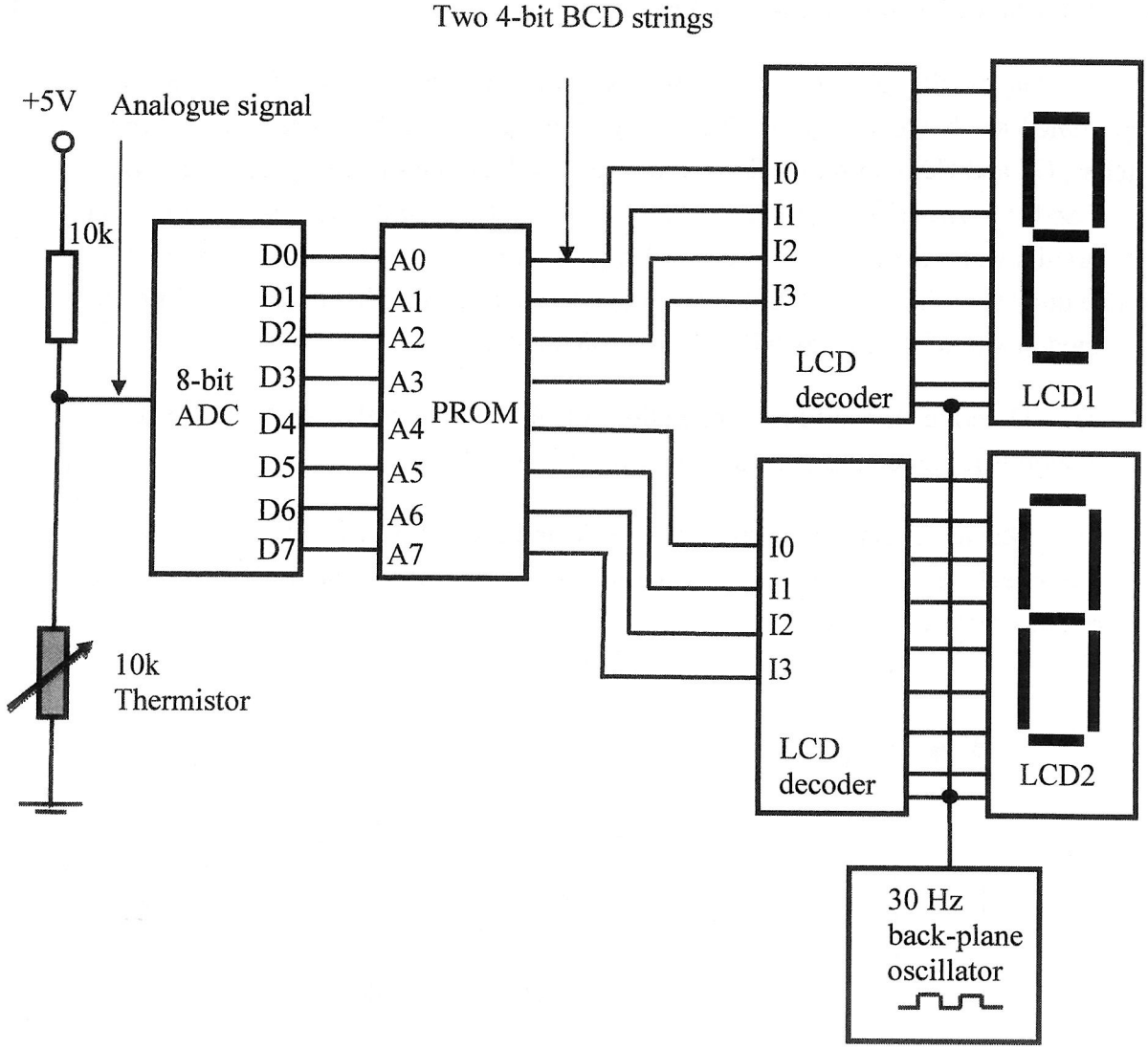

Fig. 3

(TURN OVER

4. a) Briefly discuss the advantages and disadvantages of implementing logic functions with *ROMs, Multiplexers* and *PLAs* . [20%]

(b) A macro-cell, part of a complex combinational/sequential *PAL* has been programmed as shown in Fig. 1. The binary gate signals on the *n-channel* MOSFET switches, G1 and G2, control the 2-1 multiplexers and the non-inverting tri-state buffers B1, B2 and B3. The tri-state buffers act as short-circuits when the control is 'high' and open-circuits when the control is 'low'. There are two main inputs labelled X and Y and one output labelled O1. The I/O2 pin can be configured either as an extra input or the second output of the macro-cell. The bistable is of **T** type.

(i) Describe the multiple operation of the macro-cell and find the logic functions for all combinations of the gate signals G1 and G2. [40%]

(ii) Derive the state table and the state diagram if the macro-cell is operated as a state-machine. Of what type of architecture is the state-machine? State the reasons for your answer. [40%]

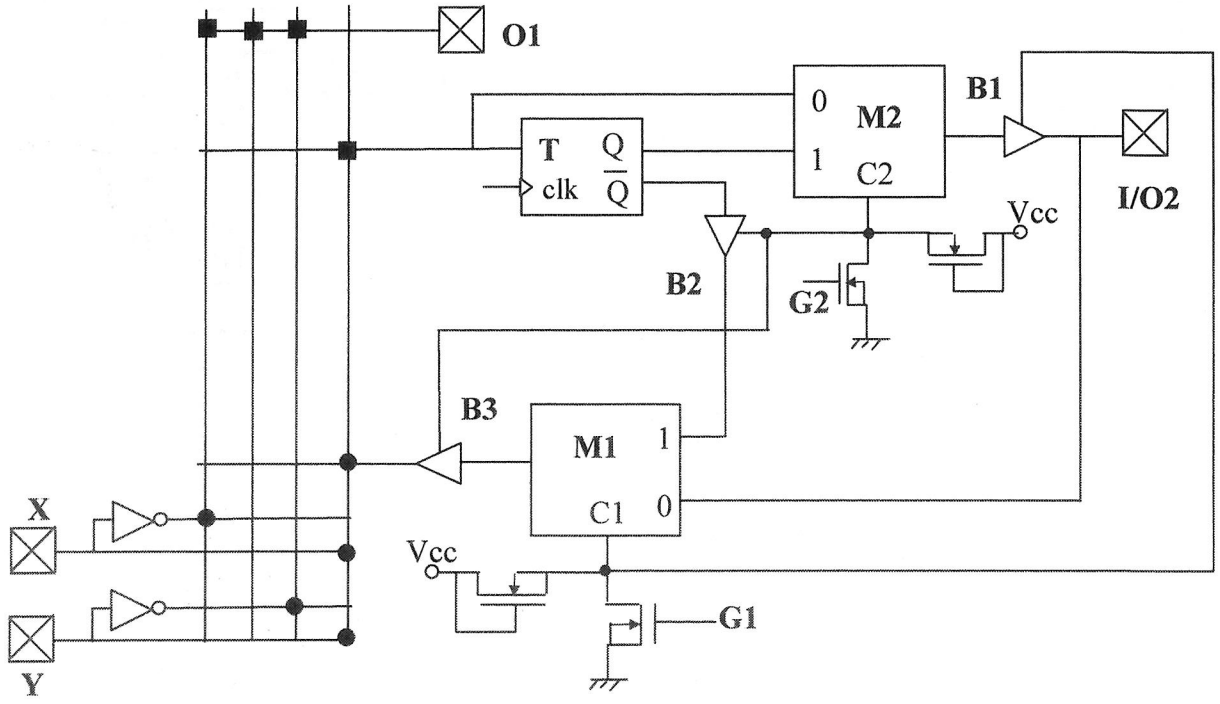

Fig. 1

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