Version DP/3

EGT2
ENGINEERING TRIPOS PART IIA

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Tuesday 04 May 2021   9.00 to 10.40

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Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet and at the top of each answer sheet.*

STATIONERY REQUIREMENTS
Write on single-sided paper.

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed.
You are allowed access to the electronic version of the Engineering Data Books.

10 minutes reading time is allowed for this paper at the start of the exam.

The time taken for scanning/uploading answers is 15 minutes.

Your script is to be uploaded as a single consolidated pdf containing all answers.

1   (a)   Explain how flash Electrically Erasable Programmable Read-Only Memory (EEPROM) (simply called flash memory, an invention that has revolutionized consumer electronics) works. Use a diagram illustrating the floating gate. Describe how a bit in the memory is programmed.   [20%]

(b)   Consider the VHDL code in Fig. 1. Given the relationship between the signals IN and OUT, what is the functionality of the circuit described by the code? Comment on whether or not this code represents a good style to use for the functionality that it represents.   [20%]

(c)   Given a 100-MHz clock signal, derive a circuit using bistables to generate 50-MHz and 25-MHz clock signals. Draw a timing diagram for all three clock signals, assuming reasonable delays.   [20%]

(d)   Analyse the circuit shown in Fig. 2.

(i)   Write the state table and sketch the state diagram.   [20%]

(ii)   Describe in words what the circuit does and comment on possible applications.   [20%]

```
library IEEE; use IEEE.STD_LOGIC_1164.all;
entity Q1 is
      port (Input: IN STD_LOGIC_VECTOR(3 DOWNTO 0);
            Output: OUT STD_LOGIC_VECTOR(3 DOWNTO 0));
end;
architecture synth of Q1 is
begin
      with Input select
            Output <= "0001" WHEN "0101",
                      "0010" WHEN "0110",
                      "0011" WHEN "0111",
                      "0010" WHEN "1001",
                      "0100" WHEN "1010",
                      "0110" WHEN "1011",
                      "0011" WHEN "1101",
                      "0110" WHEN "1110",
                      "1001" WHEN "1111",
                      "0000" WHEN OTHERS;
      end;
```
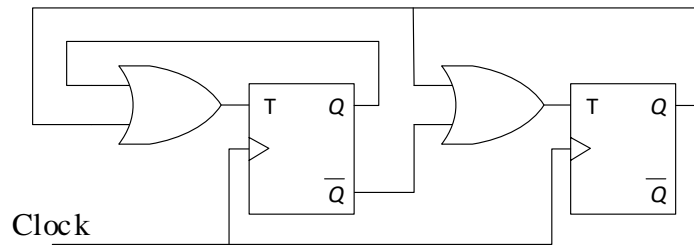Fig. 1

Fig. 2

2   (a)   Discuss the advantages and disadvantages of describing logic circuits with Finite State Machines (FSMs) and Algorithmic State Machines (ASMs).   [20%]

(b)   Consider the function $f = x_2 + \overline{x_1}\,\overline{x_3}$. Show how repeated application of Shannon's expansion can be used to derive the minterms of f.   [30%]

(c)   An FPGA Configurable Logic Block (CLB) has two four-input LUTs (G-LUT and F-LUT), and one three-input LUT (H-LUT), as shown in Fig. 3.

   (i) Give an example of a nine-input function that can be performed using only one FPGA CLB.   [10%]

   (ii) Give an example of an eight-input function that cannot be performed using only one CLB.   [10%]

(d)   Specify the size of a ROM that you could use to program the following two combinational circuits:

   (i)   A 16-bit adder/subtractor with C_{IN} and C_{OUT},   [10%]

   (ii)   An 8 x 8 multiplier.   [10%]

(e)   Is using a ROM to implement the functions in question 2 (d) a good design choice? Explain why or why not.   [10%]

Fig. 3

3   (a)   There has been an increase in multi-core processors in the last decade. Why do you think that is?   [15%]

(b)   A biological Field-Effect Transistor (bioFET) is a transistor which converts molecular signals to electrical signals. The gate current is driven by molecules incident to the gate. A logic gate is constructed using a bioFET, which has the concentration values at the gate and their corresponding output voltages given in Table 1.

     (i) Estimate values for C_{IL} and C_{IH}, which are the largest input concentration recognized as logic zero and the smallest input concentration recognized as logic one respectively.   [10%]

     (ii) Estimate values for V_{OL} and V_{OH}.   [10%]

     (iii) Estimate the logic swing.   [5%]

(c)   Consider the Transistor-transistor logic (TTL) NAND Gate shown in Fig. 4.

     (i) What do you think is the function of D_1? Explain.   [15%]

     (ii) Is there any place in the circuit where we can move D_1 to?   [15%]

     (iii) Can we replace D_1 with a resistor? What are the disadvantages of using a resistor instead of a diode in position of D_1?   [15%]

     (iv) How does decreasing or increasing R_3 affect the circuitry? Discuss.   [15%]

Table 1

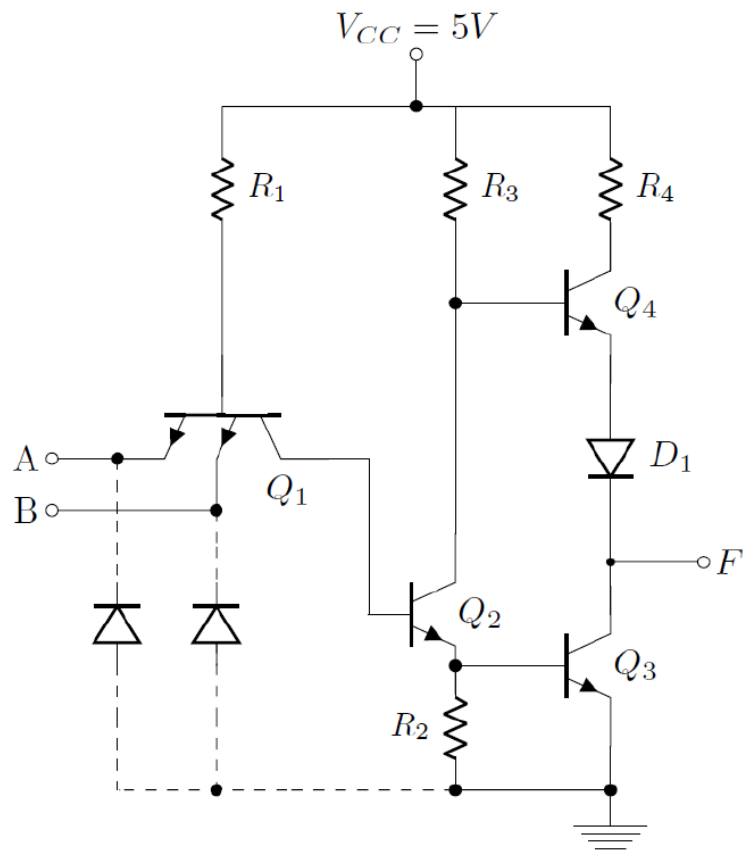| Concentration (M)	Output Voltage (V)
0.0	5.0
0.5	4.9
1.0	4.2
1.5	3.0
2.0	1.7
2.5	0.6
3.0	0.5
3.5	0.5

Fig. 4

4   The NMOS and PMOS transistors shown in Fig. 5 are matched with

$k_n' \dfrac{W_n}{L_n} = k_p' \dfrac{W_p}{L_p} = 1$ mA/V^2, $V_{Tn} = -V_{Tp} = 1$ V, $V_{DD} = 5$ V and $V_{EE} = 0$ V.

(a)   What function, $f(a,b,c)$, does this circuit implement? Find the most simplified expression for $f(a,b,c)$ and explain your answer.   [40%]

(b)   Consider a resistive load of $R_L = 1$ kΩ is connected to the output and $a = 0$ V, $b = 5$ V and $c = 0$ V are applied to the circuit. Derive the electric current passing through the load assuming $\lambda = 0$ for all transistors.   [40%]

Use the following equations for the n-channel devices:

Linear region: $I_{DS} = \dfrac{k_N}{2}[2(V_{GS} - V_{Tn})V_{DS} - V_{DS}^2]$, $V_{DS} < (V_{GS} - V_{Tn})$

Saturation region: $I_{DS} = \dfrac{k_N}{2}(V_{GS} - V_{Tn})^2$, $V_{DS} \geq (V_{GS} - V_{Tn})$

And the following equations for the p-channel devices:

Linear region: $I_{SD} = \dfrac{k_P}{2}[2(V_{SG} - |V_{Tp}|)V_{SD} - V_{SD}^2]$, $V_{SD} < (V_{SG} - |V_{Tp}|)$

Saturation region: $I_{SD} = \dfrac{k_P}{2}(V_{SG} - |V_{Tp}|)^2$, $V_{SD} \geq (V_{SG} - |V_{Tp}|)$

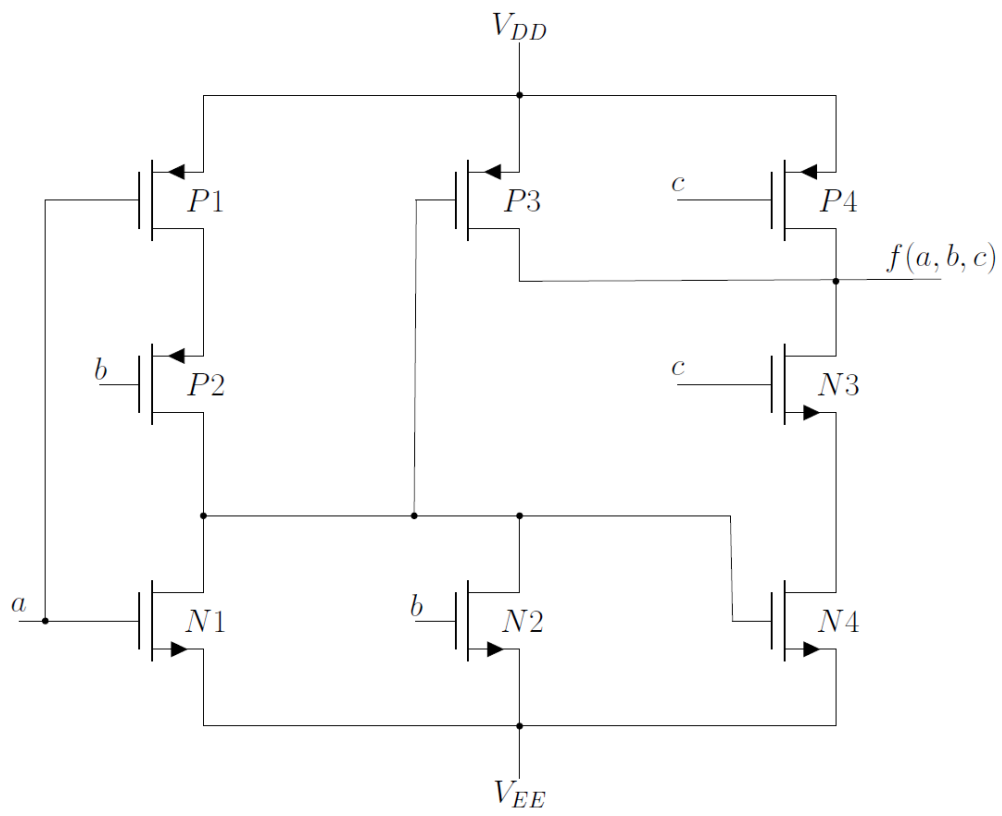(c)   For which input(s), *i.e.*, a, b, c, is the propagation delay maximum? Explain your answer.   [20%]

Fig. 5

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