Version TL/2

EGT3
ENGINEERING TRIPOS PART IIA

Tuesday 24 April 2018 2 to 3.40

Module 3B3

SWITCH-MODE ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) A single phase rectifier is shown in Fig 1.

(i) Sketch the smoothing capacitor voltage waveform and the input current waveform for a constant current load. [10%]

(ii) Explain why this rectifier has a poor power factor at the input. [15%]

(iii) Find the simplified expression for the ripple voltage in terms of the supply frequency, stating your assumptions. [15%]

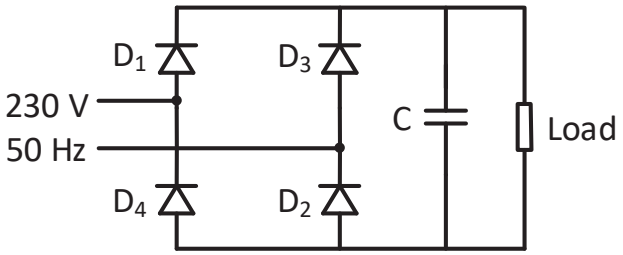

Fig. 1: Single phase rectifier

(b) A three phase rectifier is shown in Fig 2. The load current is smooth with a DC value of 100 A.

(i) Estimate the smoothing capacitance required to reduce the output ripple voltage to 5% of the peak rectified voltage for an AC line voltage of 415 V. [20%]

(ii) The ripple voltage at the output is to be reduced to 1% of the peak rectified voltage by adding a smoothing inductor. Sketch the circuit with the smoothing inductor and find the inductance. [25%]

(iii) Comment on the expected input current waveform and power factor when adding a smoothing inductor. [15%]

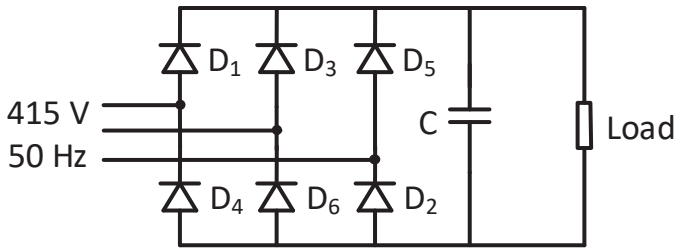

Fig. 2: Three phase rectifier

2 A Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is used to switch an inductive load as shown in Fig 3. The gate-drain capacitance of the MOSFET can be considered constant at 50 pF and the conduction resistance R_{DSon} is 7 mΩ. The MOSFET drain current I_D obeys $I_D = 150(V_{GS} - 2)^2$ where V_{GS} is the gate to source voltage. The application requires a switching frequency of 100 kHz when $V_{dc} = 100V$. The drain current I_D is 75 A and the duty cycle is 50%. The total switching time is 50 ns.

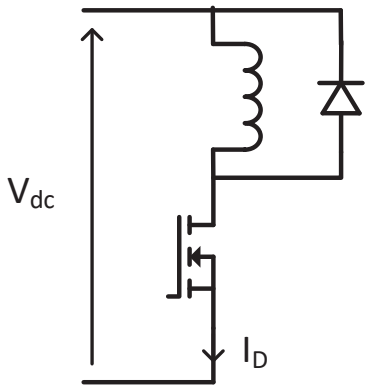

Fig. 3: MOSFET in a circuit

(a) (i) Explain why a diode is necessary for this circuit to work and state the minimum current and voltage ratings and type of diode to be used. [20%]

(ii) Estimate the total power losses, assuming an ideal diode and the MOSFET turn-on loss is assumed to be the same as the turn-off loss. [20%]

(iii) Sketch the MOSFET drain to source voltage V_{DS} and drain current I_D for a turn-off event and find a value of gate resistance which gives a 20 ns rise time of V_{DS} if the gate driver applies 0 V at turn-off. Assume an ideal diode is used. [20%]

(iv) Sketch the waveform for the MOSFET V_{DS} and I_D at a turn-off event with a non-ideal diode. [20%]

(b) A gate voltage clamp circuit is proposed, which applies a dead short between the gate and source as soon as the end of the voltage rise is detected. List two reasons why this is a good idea particularly for use in inverter circuits and give one drawback. [20%]

3 (a) Draw a non-isolated step-up-step-down DC/DC converter with using one MOSFET, one diode and one capacitor. The load is a resistor. Indicate the input voltage V_1, output voltage V_2, input current I_1, output current I_2 and the inductor current I_L on the drawing. [10%]

(i) Derive the expression of the output voltage V_2 as a function of the duty ratio D and input voltage V_1, assuming ideal devices and continuous inductor current. [10%]

(ii) At the steady state, sketch both the inductor voltage V_L and the inductor current I_L against time. [10%]

(iii) Explain the disadvantage of this converter from the perspective of earthing and input power measurement. [10%]

(b) A fly-back converter is shown in Fig 4. The flyback converter is fed by an ideal battery and the load is a resistor.

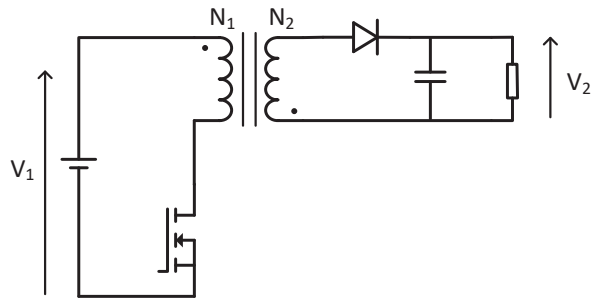

Fig. 4: Flyback converter

(i) Derive the expression of the output voltage V_2 as the function of duty ratio D and input voltage V_1, assuming ideal devices and continuous flux of the transformer. [15%]

(ii) Sketch the flux of the transformer ϕ against time, the current at the MOSFET I_s against time and the current at the diode I_d against time. [15%]

(iii) Explain why the flux of the transformer at the boundary continuity, i.e. just continuous, is preferable for the flyback converter. [10%]

(iv) The input voltage is 150 V and output voltage is 50 V. The duty ratio of the MOSFET is 50%. The load is 25 Ω. The transformer has 60 turns at the primary side, $N_1 = 60$, and the magnetising inductance, L_m, is 1 mH. If the output voltage is 50 V, determine the turns of the secondary side of the transformer, N_2, and the preferable switching frequency of the MOSFET. Ignore all losses of the converter. [20%]

4 A half-bridge power module is shown in Fig 5.

(a) Using one half-bridge with one inductor and one capacitor as a boost converter to feed a resistive load,

(i) Draw the circuit and explain the operation of switches. Derive the expression of the output voltage V_2 as the function of duty ratio D and input voltage V_1, assuming ideal devices and continuous inductor current. [20%]

(ii) Derive the expression of the load current to achieve boundary inductor current continuity when the output voltage V_2 is fixed. [10%]

(b) Using two half-bridges to build a DC to AC inverter,

(i) Draw the circuit (without AC filter). Explain the switching principle of bipolar switching and unipolar switching and state the advantage of unipolar switching over bipolar switching. [10%]

(ii) Using square wave modulation, sketch the output AC voltage against time and derive the expression of fundamental AC voltage amplitude for bipolar switching and unipolar switching, respectively. [20%]

(iii) The switching of a non-ideal device can be delayed, which can cause device failure when both upper and lower devices in a half-bridge are used. Explain the consequence of this failure caused by switching delay and the method of using gate signal to avoid such failure. State one drawback of this method. [10%]

(c) Using three half-bridges to build a DC to AC inverter feeding a three phase grid from an ideal 800 V battery,

(i) Draw the circuit. Sketch the line voltage harmonic spectrum when sine Pulse Width Modulation (PWM) is used. The switching frequency is f_s and fundamental frequency is f_1. [10%]

(ii) Determine the maximum Root Mean Square (RMS) value of the line voltage if using sine PWM and using space vector PWM, respectively. [10%]

(iii) Explain one method of reducing the size of the AC filter connecting the output of the inverter and the grid. State the main drawback of this method. [10%]

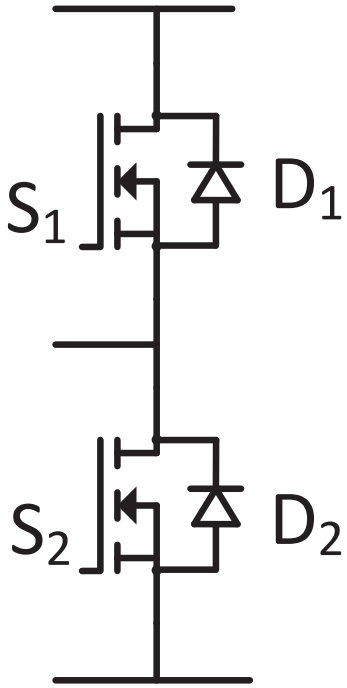

Fig. 5: Half-bridge module

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