Version TL/3

EGT3
ENGINEERING TRIPOS PART IIA

Tuesday, 03 May, 2022 2 to 3.40

Module 3B3

SWITCH-MODE ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper.

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed.
Engineering Data Book.

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 The circuit schematic of a motor drive is shown in Fig.1. The input of the motor drive is connected to the grid with negligible internal impedance. The DC link voltage is V_{dc}, the RMS value of the inverter output line voltage is V_{LL} and the DC-AC inverter of the drive uses Sinusoidal Pulse Width Modulation (SPWM),

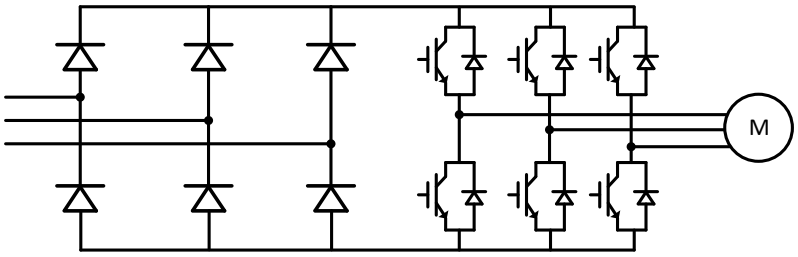

Fig. 1: Motor drive circuit schematic

(a) Derive the modulation index of SPWM in case of linear modulation. Derive the maximum line voltage if the non-linear modulation is allowed. [20%]

(b) Make comparison between the linear and non-linear modulation of the inverter in terms of output voltage, harmonics, and switching frequency. [10%]

(c) If the grid line voltage is 400 V, 50 Hz, calculate the average DC link voltage V_{dc}. [10%]

(d) If the combined inverter and motor can be represented as equivalent to a resistor with resistance R, sketch the drive input phase voltage and current. [20%]

(e) Derive the drive input current magnitude. [20%]

(f) If a large DC link capacitor is connected, sketch the DC link voltage waveform and comment on the power factor of the drive. [20%]

2 (a) Draw the cross-section structure of a power MOSFET, the current flow lines in the on-state and the depletion region associated with the JFET region. Explain the parasitic JFET effect. Show on a separate cross-section of the power MOSFET the location of the equivalent series resistances when the power MOSFET is operated as a switch in the on-state. [30%]

(b) Explain how the magnitude of these series resistances (or specific series resistances) will change if the power MOSFET is made of Silicon Carbide instead of Silicon. [30%]

(c) A power device is formed of an IGBT rated for 1.2 kV placed in parallel with a MOSFET rated for 600 V. Assume that gate terminal is common and that the IGBT and the MOSFET have the same threshold voltage and same surface area. The cathode of the IGBT is connected to the source of the MOSFET and the anode of the IGBT is connected to the drain of the MOSFET.

(i) Briefly analyse the behaviour of the power device in terms of breakdown voltage and leakage current during the off-state (blocking mode). [20%]

(ii) Describe briefly the operation of the power device during the reverse conducting mode (the current flowing from the source/cathode terminal of the power device to the drain/anode terminal of the power device). Assume that in this mode the gate is shorted to the source/cathode terminal. [20%]

3 (a) A half-bridge comprises two power MOSFETs as shown in Fig.2. This half-bridge is used for a Buck converter with an inductor L, one input capacitor C_1 and one output capacitor C_2.

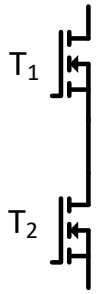

Fig. 2: Half-bridge using two MOSFETs

(i) Sketch the circuit schematic of the Buck converter. In critical continuous conduction mode, sketch the gate signal waveforms of MOSFET T_1 and T_2, and the inductor current. Mark the deadtime on your sketch and state the purpose of deadtime. [20%]

(ii) The MOSFET T_2 will have lower switching losses than T_1. Explain the cause of this switching loss reduction (hint: the MOSFET has a parasitic device engaged during deadtime). [20%]

(b) A full-bridge Buck-Boost converter is shown in Fig.3. In Boost mode, the output voltage V_o is larger than the input voltage V_i. In Buck mode, the output voltage V_o is smaller than the input voltage V_i. The deadtime is neglected.

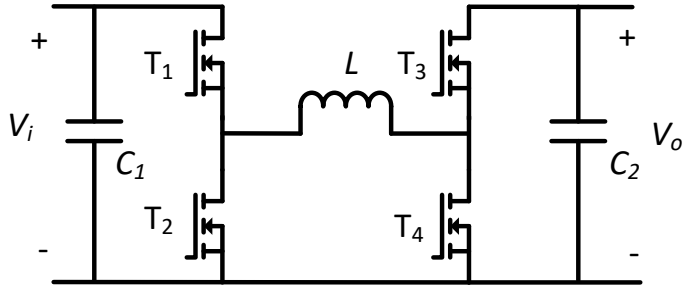

Fig. 3: Full-bridge Buck-Boost converter

(i) In Buck mode, the inductor current i_L is continuous. Derive the voltage transfer ratio $\frac{V_o}{V_i}$ and sketch the waveforms of the gate signal of MOSFETs. [30%]

(ii) In Boost mode, the inductor current i_L is continuous. Derive the voltage transfer ratio $\frac{V_o}{V_i}$ and sketch the waveforms of the gate signal of MOSFETs. [30%]

4 (a) The circuit schematic of a Flyback converter is shown in Fig.4. The input voltage of this Flyback converter is V_1 and the output voltage is V_2. The number of turns of the primary and secondary winding is N_1 and N_2, respectively. The magnetising inductance of the transformer is L_m. The duty cycle of the transistor of the Flyback converter is D. The circuit is considered as lossless and all voltage ripples are neglected.

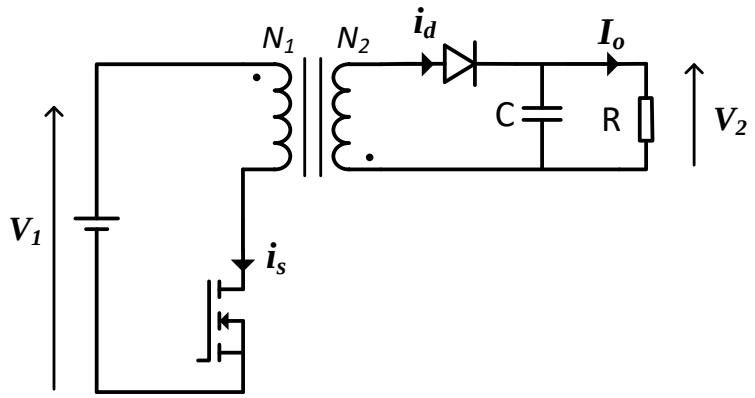

Fig. 4: Flyback converter circuit schematic

(i) Derive the expression of the output voltage V_2 when the flux of the transformer core is continuous. [20%]

(ii) The input and output voltage of the Flyback is 400V and 40V, respectively. The output current is 10 A. If the transistor of the Flyback converter is required to operate at 100 kHz and a 50% duty ratio, calculate the minimum magnetising inductance of the transformer in this Flyback converter. [30%]

(b) The circuit schematic of a half-bridge LLC converter is shown in Fig.5. The input voltage of this LLC converter is V_i and the output voltage is V_o. The number of turns of the primary and secondary winding is N_1 and N_2, respectively. The magnetising inductance of the transformer is L_m. The duty cycle of the half-bridge is 50%. The resistive load has the resistance as R. An inductor L_r and a capacitor C_r have been used as a resonant tank. The circuit is considered as lossless and all voltage ripples are neglected.

(i) Define the switching frequency of the half-bridge when this LLC converter operates at the resonant frequency. [10%]

(ii) Derive the voltage gain $\frac{V_o}{V_i}$ with respect of switching frequency when L_m is much larger than L_r (hint: the rectifier side resistance can be equivalent as $\frac{8R}{\pi^2}$). [20%]

(iii) Sketch the waveform of output voltage of the half-bridge v_r and current i_r when operating at the resonant frequency. [20%]

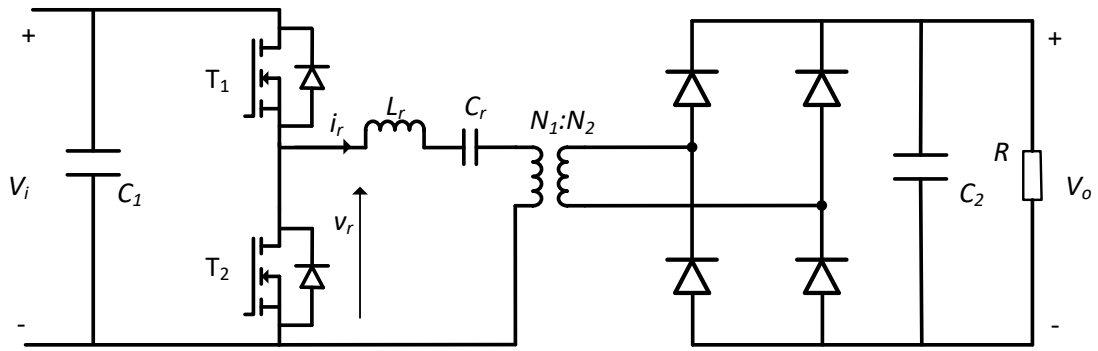

Fig. 5: Half-bridge LLC converter circuit schematic

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1° (a) $\frac{2\sqrt{3}}{\pi} V_{dc}$

(c) 540 V

(e) $I_n = \sum_{n=1,5,7,\cdots}^{\infty} \left(\frac{\sqrt{6}}{\pi^2 n} \frac{V_{LL}}{R} \right)$

3° b (i) D

(ii) $\frac{1}{1-D}$

4° a, (i) $V_2 = \left(\frac{D}{1-D}\right) \frac{N_2}{N_1} V_1$

(ii) 500 μH

(b) (i) $\frac{1}{\sqrt{L_r C_r}}$

(ii) $\frac{1}{2} \frac{1}{\sqrt{1 + Q^2 \left(\frac{1}{\omega_n} - \omega_n\right)^2}}$, $Q = \frac{\omega L_r}{R_T}$,

$R_T = \left(\frac{N_2}{N_1}\right)^2 \frac{8R}{\pi^2}$, $\omega_n = \frac{\omega}{\omega_r}$, $\omega_r = \frac{1}{\sqrt{L_r C_r}}$

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