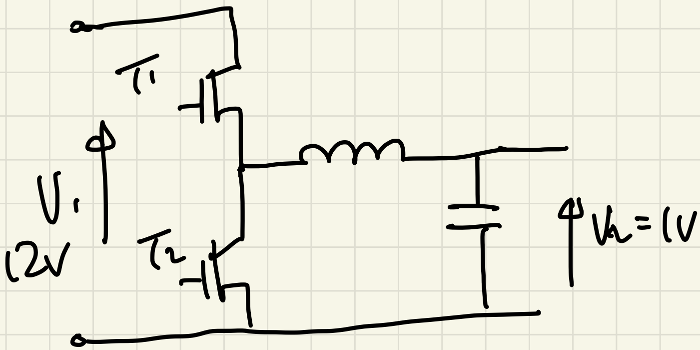
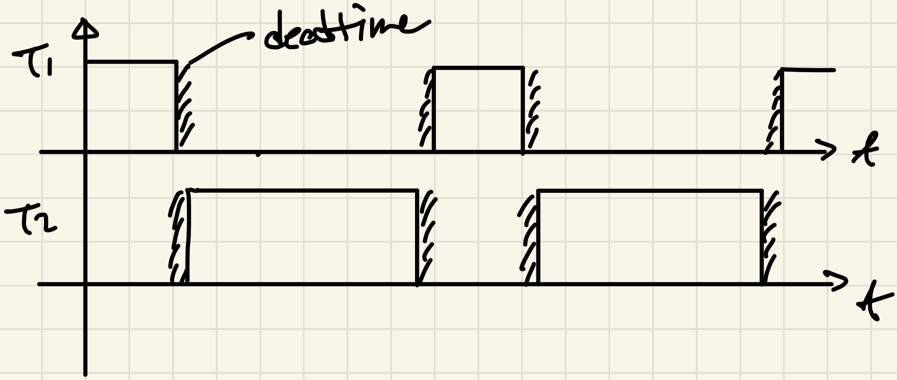
Q1

(a)





(b) T_2 has lower switching loss. The body diode of T_2 conducts current during deadtime. Therefore, when T_2 switches on after the deadtime, it has nearly zero voltage and the switching on loss is nearly zero.

(c)

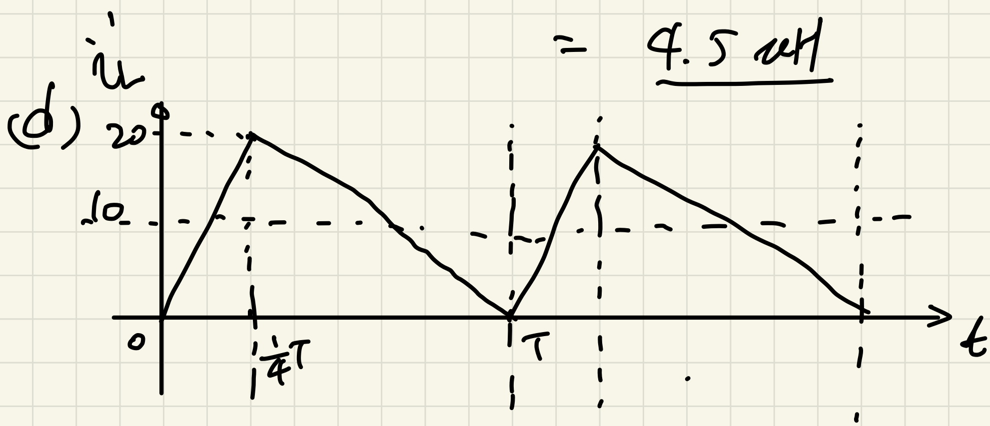
$$L\frac{\Delta i_L}{\Delta t} = V_1 - V_2 \quad , \quad L = \frac{(V_1 - V_2)\Delta t}{\Delta i_L}$$

$$= \frac{(48-12) \times \frac{1}{4} \times \frac{1}{500\times10^3}}{4}$$

$$= 4.5 \times 10^{-6}\ H$$

$$= \underline{4.5\ \mu H}$$

(d)



$$L' = \frac{(V_1 - V_2)\Delta t}{\Delta i_L'} = \frac{(48-12) \times \frac{1}{4} \times \frac{1}{500\times10^3}}{20}$$

$$= \underline{0.9\ \mu H}$$

8

(e) $0 < t < \frac{T}{4}$. T_1 conducting.

$$P_{T_1} = \frac{\int_0^{T/4} i_{T_1}^2 R\,dt}{T} = \frac{R}{T}\int_0^{T/4} \left(\frac{80}{T}t\right)^2 dt = \frac{(80)^2 R}{T^3}\,\frac{t^3}{3}\Big|_0^{T/4}$$

$$= \frac{100}{3}R = \underline{0.067W}$$

$\frac{T}{4} < t < T$, T_2 conducting.

$$P_{T_2} = \frac{\int_{\frac{T}{4}}^{T} i_{T_2}^2 R\,dt}{T} = \frac{R\int_0^{\frac{3}{4}T} \left(\frac{80}{3T}t\right)^2 dt}{T} = 100R = \underline{0.2W}$$

// Alternative: using RMS current to find the total loss.

$$P = \left(\frac{20}{3}\right)^2 \cdot R = 0.267W. \quad P_{T_1} = \frac{1}{4}P = 0.067W$$
$$P_{T_2} = \frac{3}{4}P = 0.2W$$

//

(f) CCM:

$$I = I_{DC} + I_{ripple}, \quad I_{ripple} \text{ has peak value } 2A$$

$$I_{RMS} = \sqrt{I_{DC}^2 + I_{ripple\,RMS}^2} = \sqrt{10^2 + \left(\frac{2}{\sqrt{3}}\right)^2}$$

$$P_{loss\,CCM} = I_{RMS}^2 R = \left(100 + \frac{4}{3}\right)R$$

Critical CCM

$$I = I_{DC} + I_{ripple}, \quad I_{ripple} \text{ has peak value } 10A$$

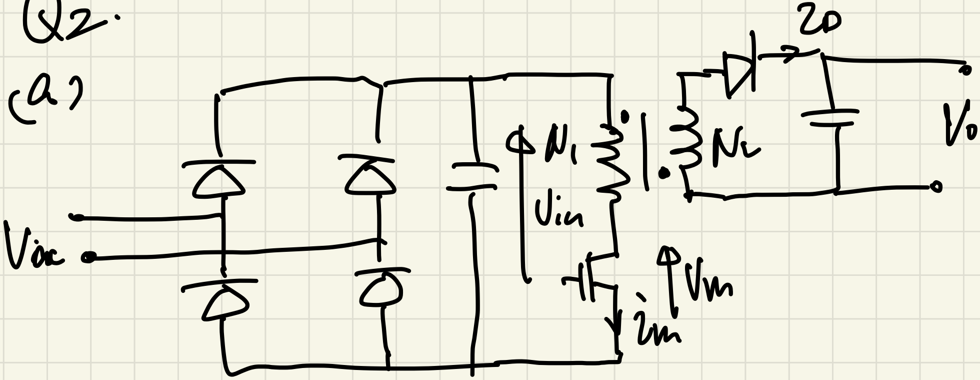
$$I_{RMS} = \sqrt{I_{DC}^2 + I_{ripple}^2} = \sqrt{10^2 + \left(\frac{10}{\sqrt{3}}\right)^2}$$

$$P_{loss\,critical\,CCM} = \left(100 + \frac{100}{3}\right)R$$

$$\frac{P_{critical\,CCM}}{P_{CCM}} = \frac{\frac{400}{3}}{\frac{304}{3}} = \underline{1.315}$$

Q2.

(a)



(b) The capacitor is very large thus the DC voltage is clamped at the peak voltage of input.

$V_{DC} = \sqrt{2} \cdot V_{ac\,rms} = \sqrt{2} \times 230 = \underline{325V}$.

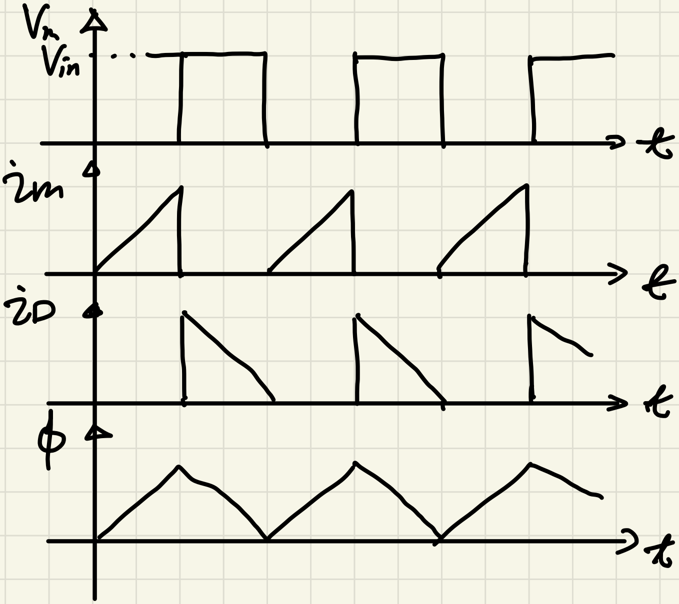
The input current is very distorted so the power factor is poor.

(c) Flux is contineous, $\frac{V_o}{V_{in}} = \frac{N_2}{N_1} \frac{D}{1-D}$

It's a step down Flyback, thus $\frac{N_2}{N_1} = \frac{1}{20}$

$\frac{D}{1-D} \cdot \frac{1}{20} = \frac{15}{325}$. $D = \underline{0.48}$

(d)



e) Max B_m is set by saturation point

$$B_m = 0.75 \times 0.36 = 0.27\ T.$$

$$\phi_m = B_m \cdot A = 0.27 \times 0.25 \times 10^{-4} = 0.0675 \times 10^{-4}\ Wb$$

$$N_1 \frac{d\phi}{dt} = V_{in}$$

$$N_1 = \frac{\Delta t\, V_{in}}{\Delta\phi} = \frac{DTV_{in}}{\Delta\phi} = \frac{0.48 \times \frac{1}{500\times10^3} \times 325}{}$$

$$= \underline{46.2 \approx 46}$$

$$N_2 = \frac{46}{20} = \underline{2.3 \approx 2}$$

Using the modified turns ration $\frac{46}{2} = 23$,

modified duty ratio $\frac{D'}{1-D'} = 23 \times \frac{15}{325}$

$$D' = 0.515$$

(f)

Assum: ① B is evenly distributed in the core

② Leakage inductance is neglected.

$$\frac{I_{2max} \cdot (1-D)T}{2} = I_2 \cdot T$$

$$I_{2max} = \frac{2I_2}{1-D} = \frac{2 \times 2}{1-0.515} = 8.25A.$$

Magnetis inductance referred to 2^{nd} side,

$$V_o = L_m \frac{\Delta \hat{i}_2}{\Delta t}, \quad L_m = \frac{V_o \Delta t}{\Delta i_2} = \frac{V_o (1-D)T}{I_{2max}}$$

$$= \frac{15 \times 0.485 \times \frac{1}{500 \times 10^3}}{8.25}$$

$$= 1.76 \times 10^{-6} H$$

$$L_m = \frac{N_2^2 \mu_0 \mu_r A}{l}, \quad \mu_r = \frac{L_m \cdot l}{N_2^2 A \mu_0}$$

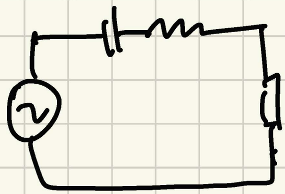
$$= \frac{1.76 \times 10^{-6} \times 10^{-2}}{2^2 \times 0.25 \times 10^{-4} \times 1.26 \times 10^{-6}}$$

$$= \underline{139.6}$$

Q3

(a) $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$

(b)

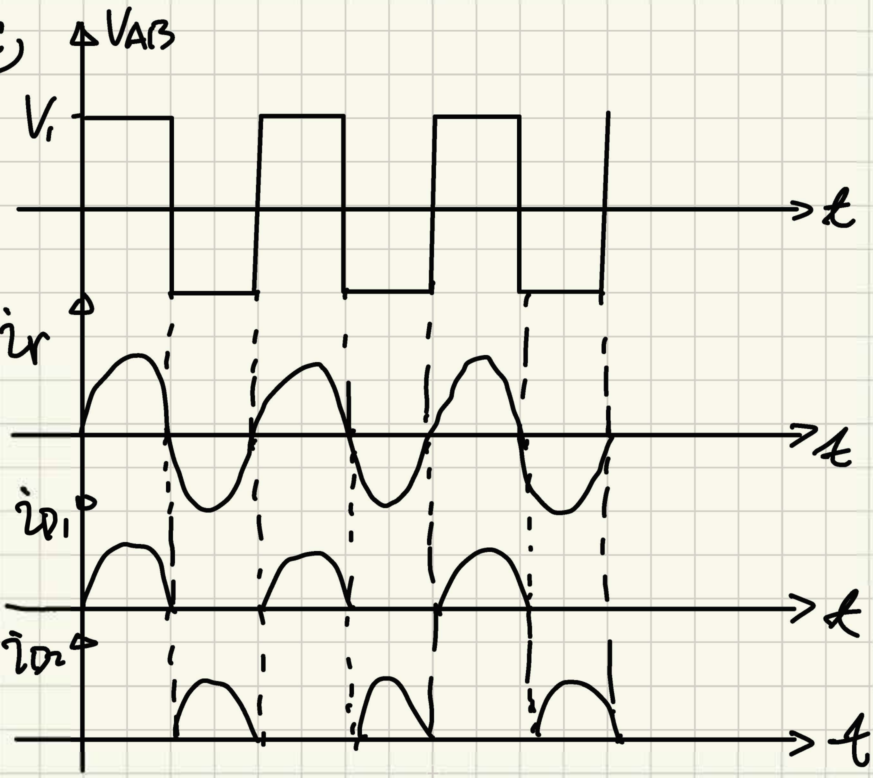


Voltage square, current sin.

$$R_s = \frac{N^2 \cdot \frac{2\sqrt{2}V_o}{\pi}}{\frac{\pi I_o}{2\sqrt{2}}} = N^2 \cdot \frac{8R}{\pi^2}$$

$$R_s = \frac{8N^2R}{\pi^2}$$

(c)



(d) The magnetizing inductance of transform is very large. At f_s, the tank impedance is zero.

therefore, $V_o = \frac{\hat{V}_{AB1}}{N} = \frac{4 V_i}{\pi N}$

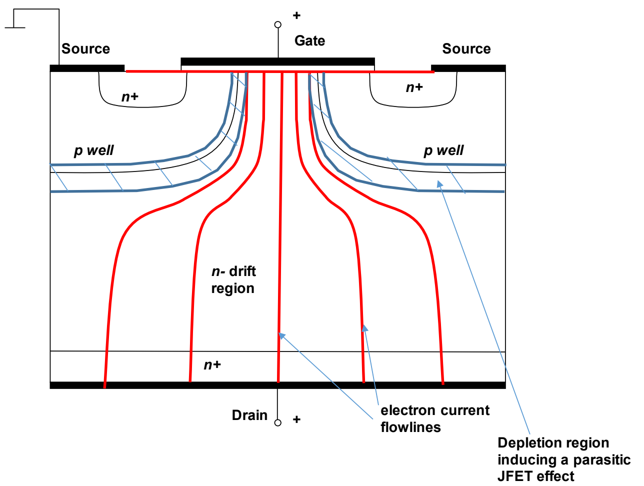
(e) In this LLC, $k = \frac{L_m}{L_r} \to \infty$.

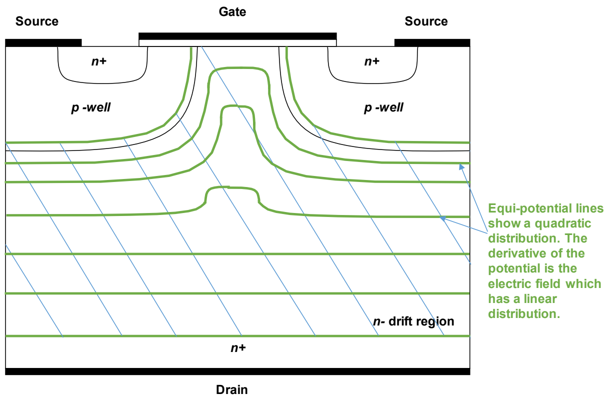
when Q is small, the gain changes insignificantly when f_s deviates from f_r.

For a given rated current, the Q can be set to be small. Then, when the load is reduced Q can only be even smaller. The chart shows the gain is becoming even smoother. Thus the gain has even smaller changes when f_s is not f_r. therefore, no matter the load change, the gain remains nearly unchanged.

Q4

a)





Flow-lines in the on-state. The electrons flow from the source terminal, the n+ source region, through the channel, the neck region, where a parasitic JFET effect is present, through the n- drift region, the n+ substrate to the drain terminal	Equipotential lines during off-state blocking. One can assume a linear distribution of the electric field and a quadratic distribution of the potential lines. In the neck region, the potential lines are not flat, but bending upwards. The bending depends on the curvature of the junction and the pitch between adjacent p-wells.

[20%]

(a)

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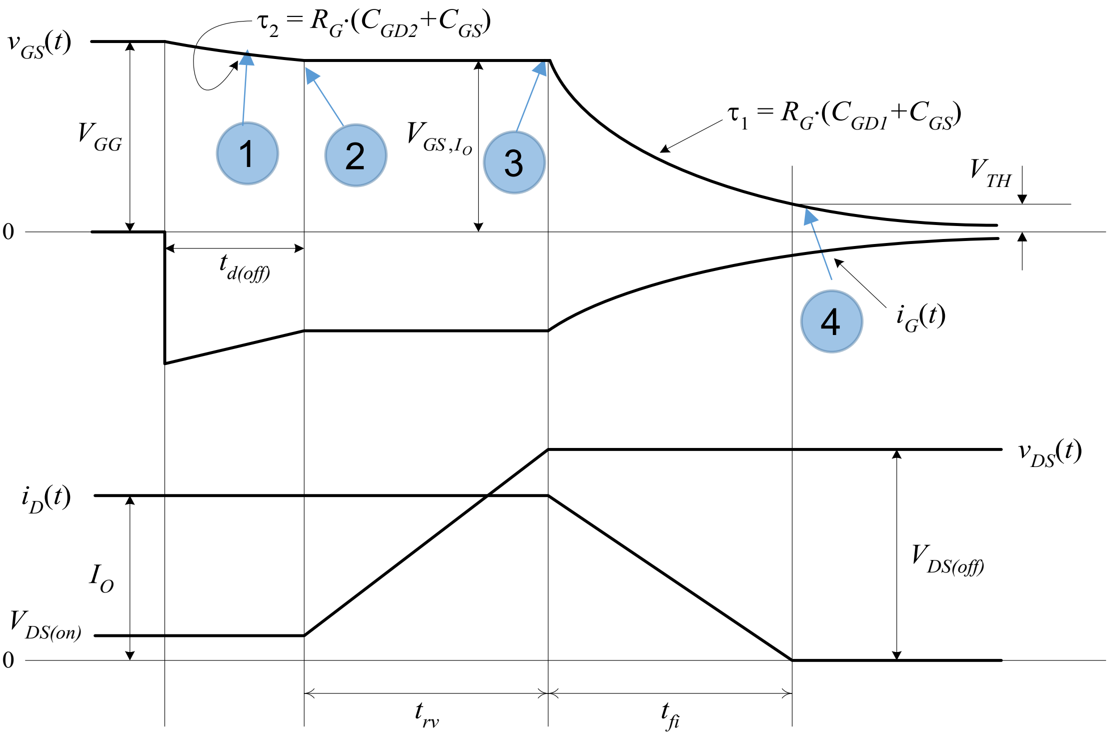
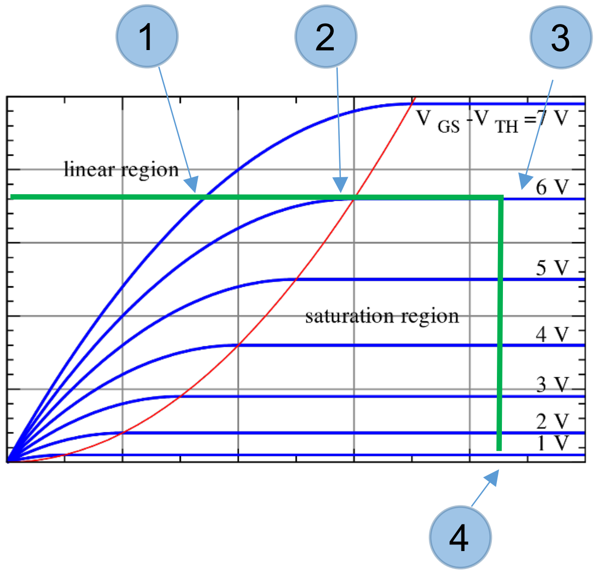
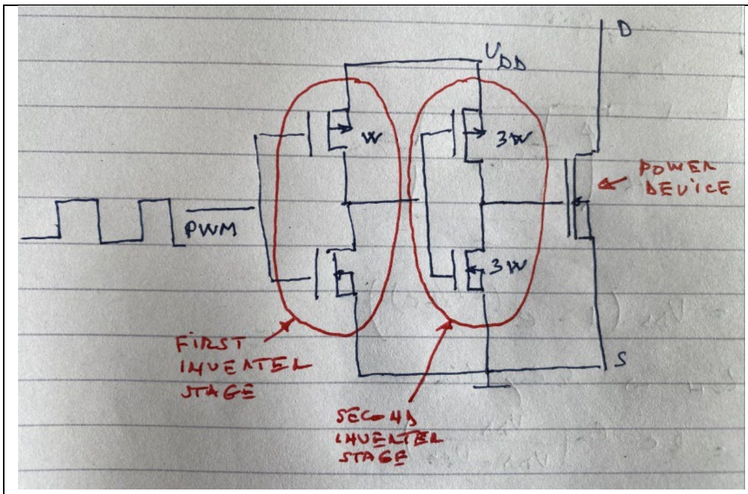




- C_{GD1} - Miller capacitance (saturation region – this capacitance is small)
- C_{GD2} - Miller capacitance (linear region –this capacitance is large)
- C_{GS} - Gate-Source capacitance
- t_{doff} - Initial delay time
- t_{rv} - Rise time in which v_{DS} reaches its off-state value $V_{DS(off)}$ from $V_{DS(on)}$.
- t_{fi} - Time taken for i_D to fall from its full load value I_o to 0; the end of this

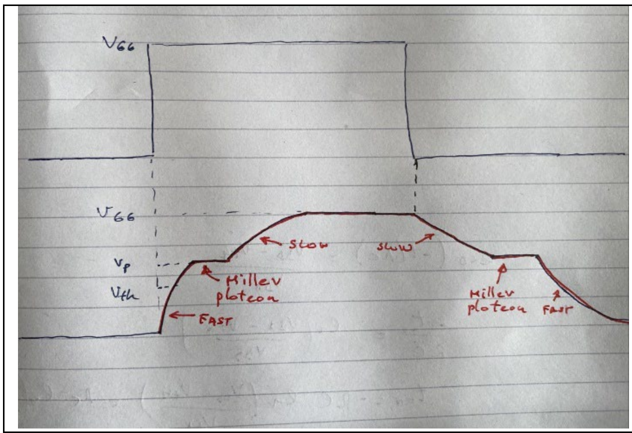
[40%]

(b)

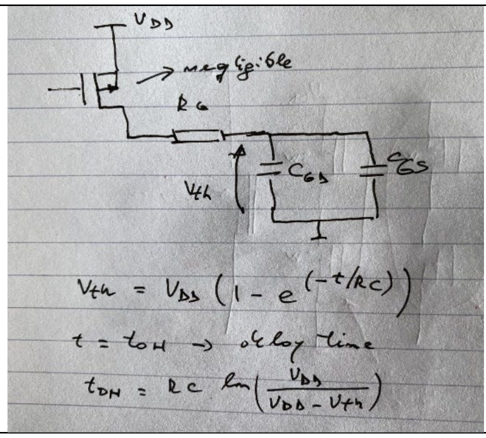


The two-stage inverters are typical CMOS with a n-channel on the low side and p-channel on the high side. The second inverter has larger transistors (e.g. 3x width or even larger) to minimise the on-state resistances of the n-channel and p-channel transistors. The gate resistance is not specifically shown, but could be internal or added between the output of the second stage and the gate of the power transistor to control the dVdt.

[15%]



The shape of the gate signal is dictated by the switching conditions (here it is shown to be inductive0 [15%]



The turn-on delay time is until the channel becomes open – Vth.
The input capacitance is the parallel combination of CGD and CGS. R=RG.
C=CGS + CGD [10%]