Version TL/3

EGT2
ENGINEERING TRIPOS PART IIA

Tuesday 02 May 2023 14:00 to 15:40

Module 3B3

SWITCH-MODE ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 A Buck converter is comprised of two power MOSFETs. The input voltage is 48V and the output voltage is 12V. The converter is operated at the rated output current of 10A and the inductor current is in continuous conduction mode (CCM). The switching frequency is 500kHz. Each MOSFET has a conduction resistance of 2mΩ.

(a) Sketch the circuit schematic of the Buck converter. Sketch the gate signal waveforms of the two MOSFETs and mark the dead time. [10%]

(b) Which of the MOSFETs has a lower switching loss and why? (Hint: the MOSFET has a parasitic device engaged during deadtime.) [10%]

(c) If the dead time is neglected, the peak to peak value of the inductor current is 4A. Calculate the inductance value and sketch the inductor current against time, neglecting the dead time and the resistance of the MOSFET and inductor. [15%]

(d) If this Buck converter is operated at the critical CCM, the inductor needs to be changed. Calculate the new inductance, neglecting dead time and the resistances of the MOSFET and the inductor. [15%]

(e) Calculate the conduction loss of each MOSFET when operating at the critical CCM, neglecting the dead time. [20%]

(f) Numerically compare the total conduction loss of the MOSFETs between the CCM in part (c) and critical CCM in part (d). (Hint: the triangle waveform RMS value equals its peak value divided by $\sqrt{3}$.) [30%]

2 A smart mobile phone charger comprises a single-phase diode bridge rectifier and a MOSFET based Flyback DC-DC converter. The input voltage is 230V and the output is 15V. The charger is operated at the rated output current of 2A. The MOSFET is operated at 500kHz. The magnetic core of the Flyback converter has a cross section area of 0.25cm^2. The saturation point of the flux density is 0.36T. The flux in the transformer is critically continuous and the peak is 25% below the saturation point. Components in this converter are considered as ideal and the converter is lossless.

(a) Sketch the circuit schematic of the charger. [15%]

(b) The output capacitance of the rectifier is very large. Calculate the input voltage of the Flyback converter and comment on the power factor of this charger. [10%]

(c) If the turns ratio of the transformer in the Flyback converter is 20, calculate the duty ratio of the MOSFET. [15%]

(d) Sketch the waveforms of the MOSFET voltage, the MOSFET current, diode current, and the magnetic flux of the Flyback converter against time. [20%]

(e) Calculate the number of turns of each winding of the transformer in the Flyback converter. Calculate the modified duty ratio. [20%]

(f) Calculate the relative permeability of the transformer core when the effective length of the core is required to be 1cm (permeability of free space is: $1.26 \times 10^{-6} H \cdot m^{-1}$). State your assumptions. [20%]

3 A LLC resonant converter is shown in Fig 1. The input and output voltages are V_1 and V_2, respectively. The output of the LLC has a large capacitor C_o. The load at the rated power is represented as R. The resonant tank has an inductor and a capacitor denoted as L_r and C_r, respectively. The transformer magnetising inductance is large. The secondary side of the transformer has two windings where the turns ratio between the primary and each secondary winding is $N : 1$. The converter is operated at the resonant frequency and the full-bridge is operated in bipolar mode. The dead time can be neglected. Components in this converter are considered as ideal and the converter is lossless.

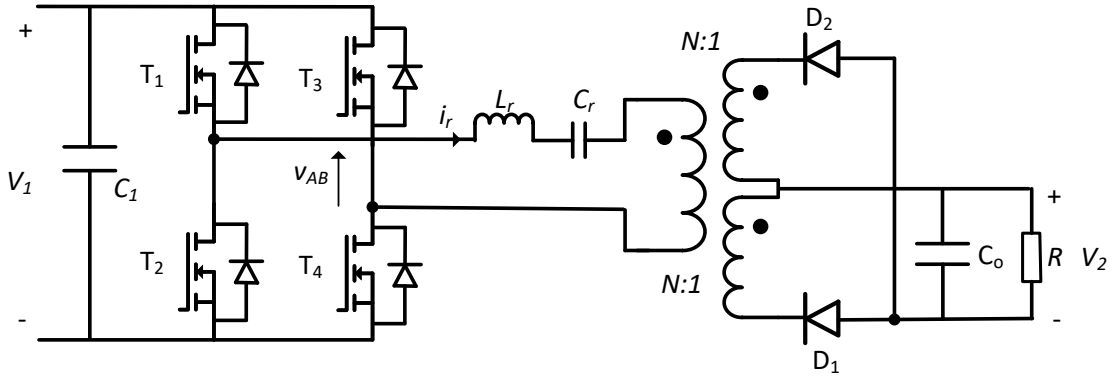

Fig. 1

(a) Define the switching frequency of the full-bridge. [10%]

(b) Derive the expression of the load power. (Hint: the transformer voltage is a square wave but the current is a sine wave when resonant). [20%]

(c) Sketch the waveform of the full-bridge output voltage v_{AB}, the current at the resonant tank i_r, the currents at D_1 and D_2 against time. [25%]

(d) Derive the expression for the voltage gain. State three benefits of this LLC converter. [25%]

(e) If the switching frequency f_s slightly deviates from the resonant frequency f_0, this LLC converter will still have the same voltage gain within the load range. Discuss the reason for this behaviour by using the chart shown in Fig 2 in which $k = L_m/L_r$. (Hint: the quality factor Q is $\left(\sqrt{\frac{L_r}{C_r}}\right)/R_s$, R_s is the equivalent resistance looking at the transformer secondary side). [20%]

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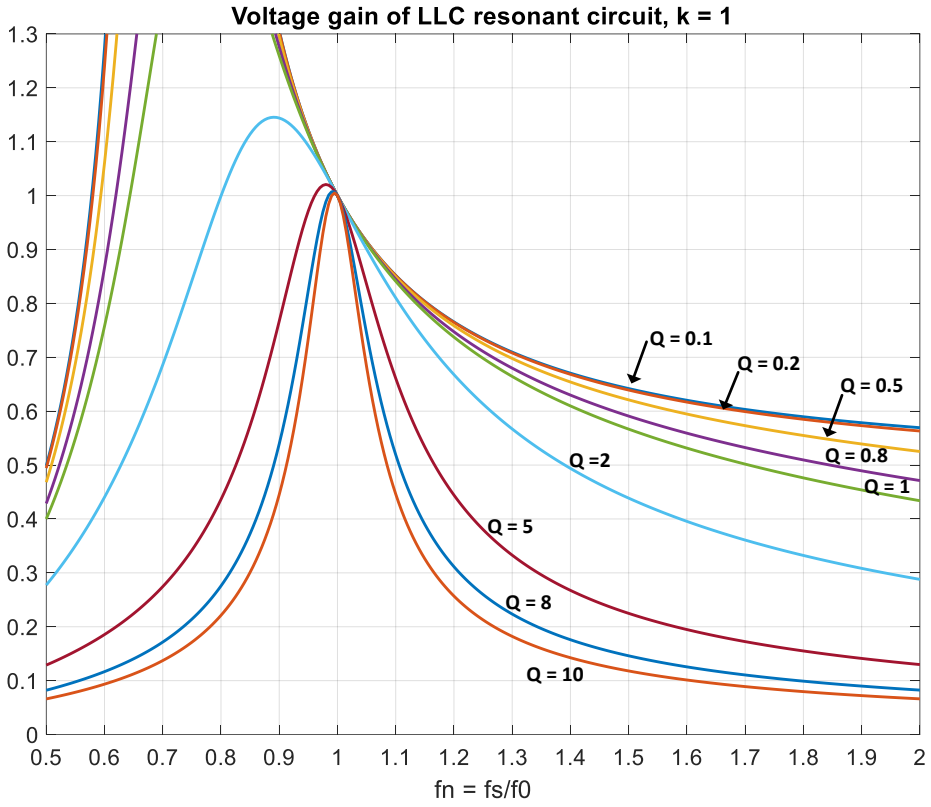
Voltage gain of LLC resonant circuit, k = 1
Q = 0.1
Q = 0.2
Q = 0.5
Q = 0.8
Q = 1
Q =2
Q = 5
Q = 8
Q = 10
fn = fs/f0

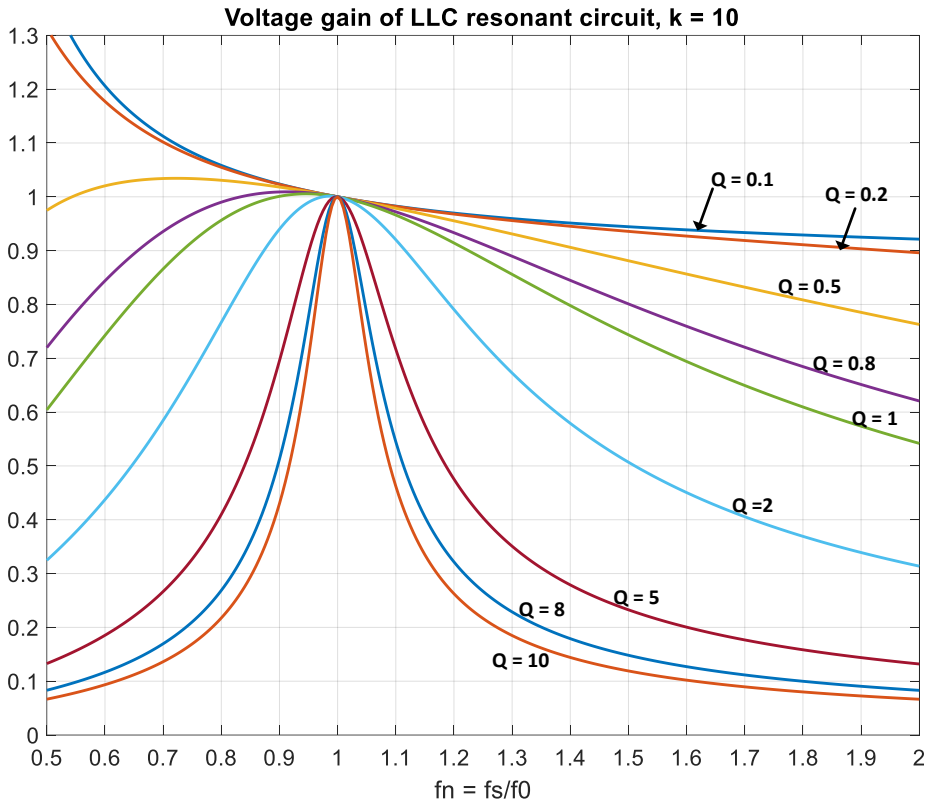
Voltage gain of LLC resonant circuit, k = 10
Q = 0.1
Q = 0.2
Q = 0.5
Q = 0.8
Q = 1
Q =2
Q = 5
Q = 8
Q = 10
fn = fs/f0

Fig. 2

4 (a) Draw the sectional structure of a Power Metal–Oxide–Semiconductor Field Effect Transistor (MOSFET) and indicate the current flow lines in the on-state and potential lines in the off-state blocking mode. [30%]

(b) Sketch the transient graphs for the gate-source voltage v_{gs}, and drain-source voltage v_{ds}, and the drain current i_d as a function of time of a power MOSFET in inductive conditions. By using the static I-V characteristics explain the various significant points in the transient characteristics. [30%]

(c) A simple gate driver for a Power MOSFET uses a double inverter stage.

(i) Draw the circuit schematic of the driver. [15%]

(ii) Assuming an ideal square wave signal at the input of the driver, sketch the shape of the signal at the gate input of the Power MOSFET. [15%]

(iii) Estimate the turn-on delay time with respect to the gate resistance, the gate-source capacitance and the gate-drain capacitance. Neglect the on-state resistances of the transistors of the double inverter stage. [10%]

END OF PAPER