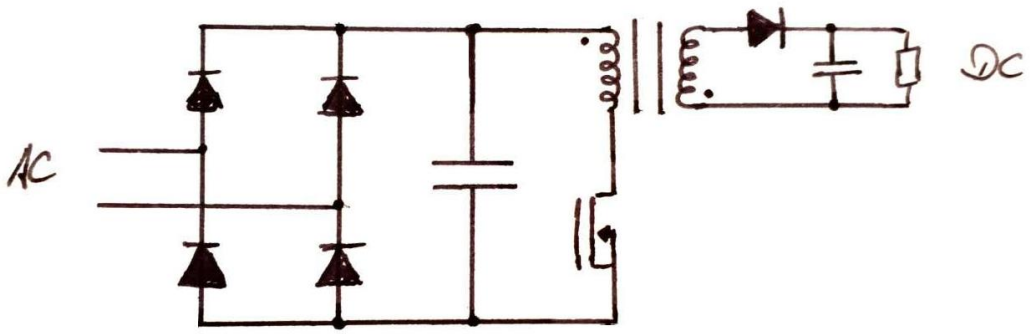
3B3, 2024 Lent

1(a)



1(b)

On: $$\Delta\Phi = \int_0^{DT} \frac{V_{\text{fb,in}}}{N_1}\,\mathrm{d}t = DT \cdot \frac{V_{\text{fb,in}}}{N_1}$$

Off: $$\Delta\Phi = \int_{DT}^{T} \frac{V_{\text{fb,out}}}{N_2}\,\mathrm{d}t = (1-D)T \cdot \frac{V_{\text{fb,out}}}{N_2}$$

$$DT \cdot \frac{V_{\text{fb,in}}}{N_1} = (1-D)T \cdot \frac{V_{\text{fb,out}}}{N_2}$$

$$\frac{V_{\text{fb,out}}}{V_{\text{fb,in}}} = \frac{N_2}{N_1}\frac{D}{1-D}$$

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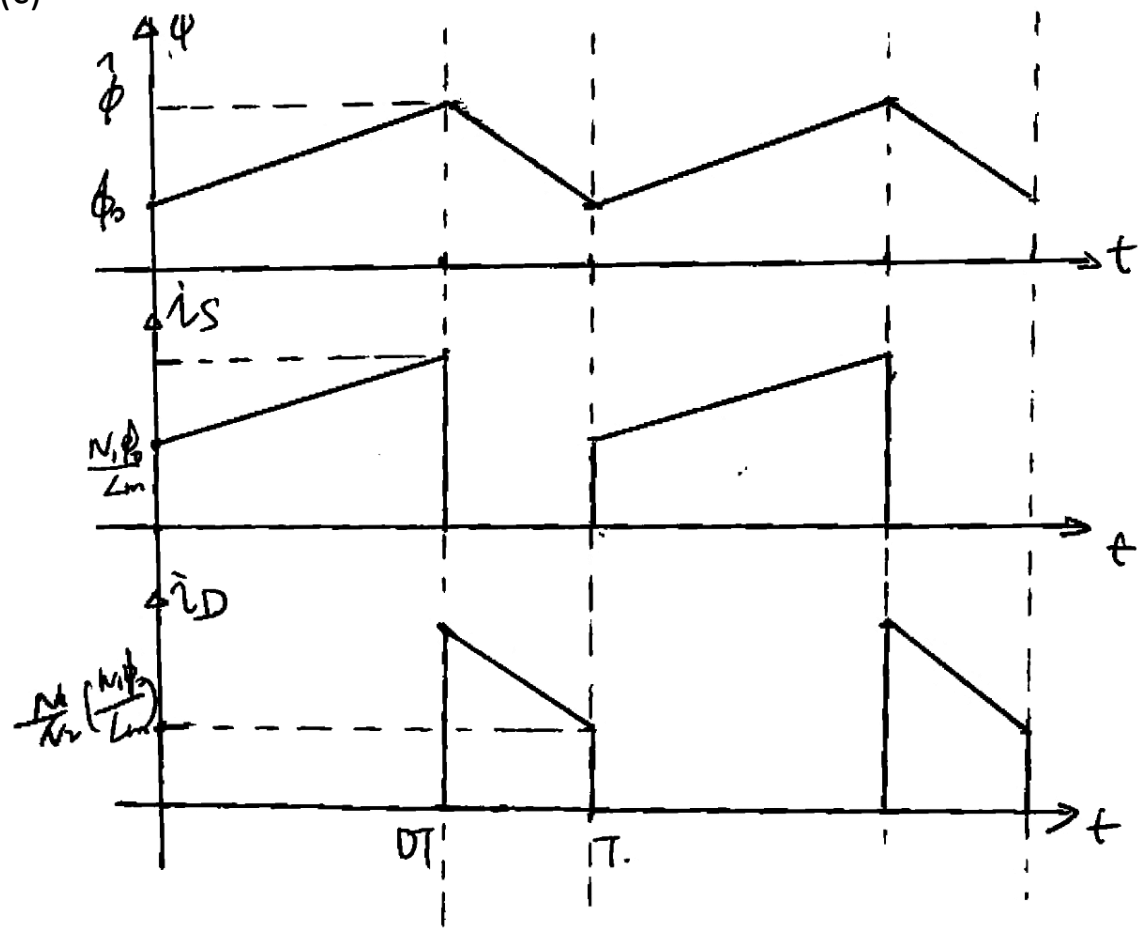
1(c)



1(d)

The core of the transformer limits the maximum flux that can be reached and therefore the power to be transferred (for a fixed frequency/cycle length). Therefore, the flux should start at its minimum, i.e., 0 or close to it, for maximum available range before saturation. Discontinuous operation, on the other hand, reduces the transferred power again.

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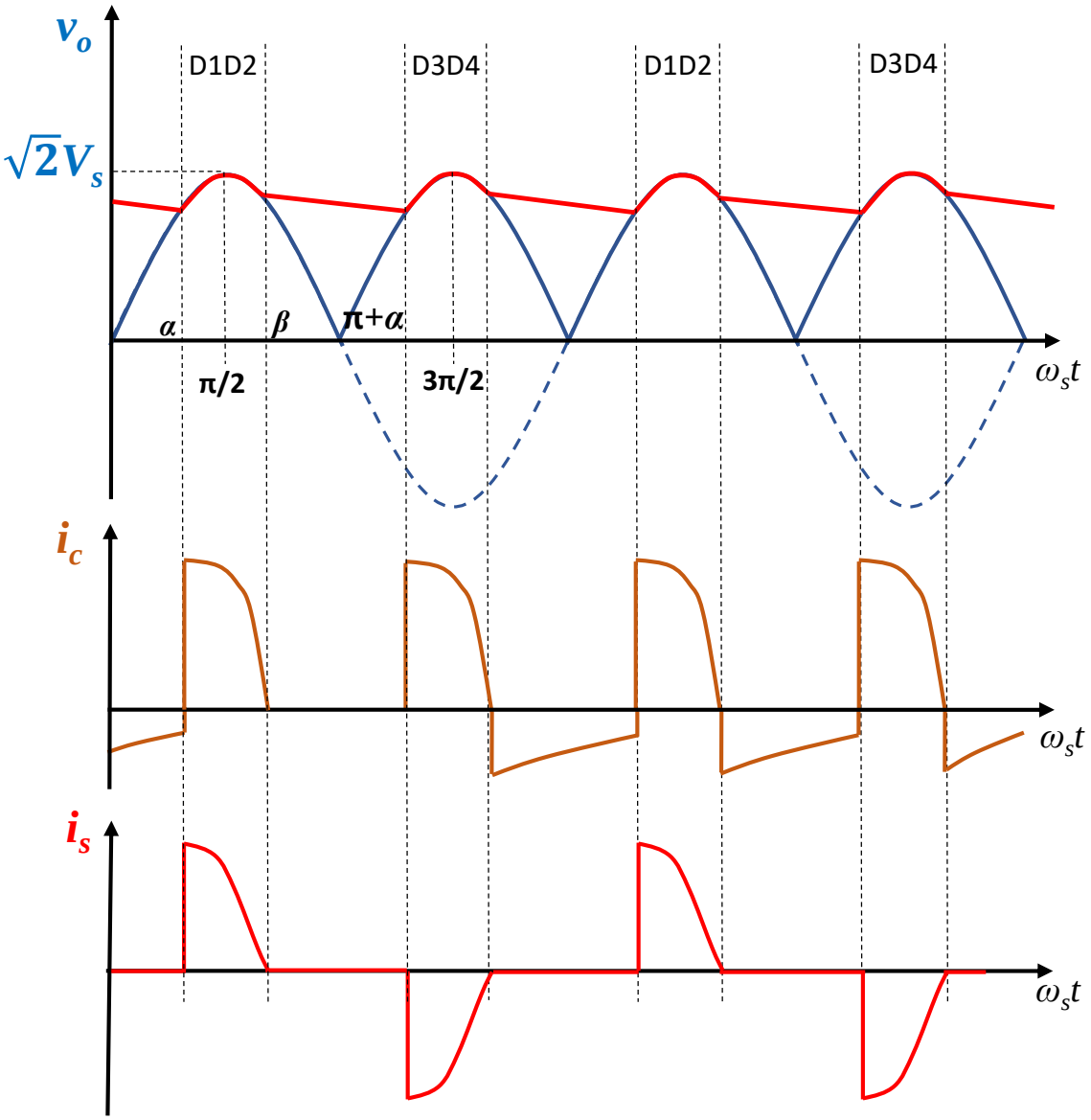
1(e)



This circuit only draws current from the mains around the peak of the voltage to top off the capacitor. There are practically only two current surges per 50 Hz period. Instead of sinusoidal load with high power factor, this power supply draws large peak currents and injects extremely high frequency content into the mains. The larger the capacitor is the more severe the problem becomes.

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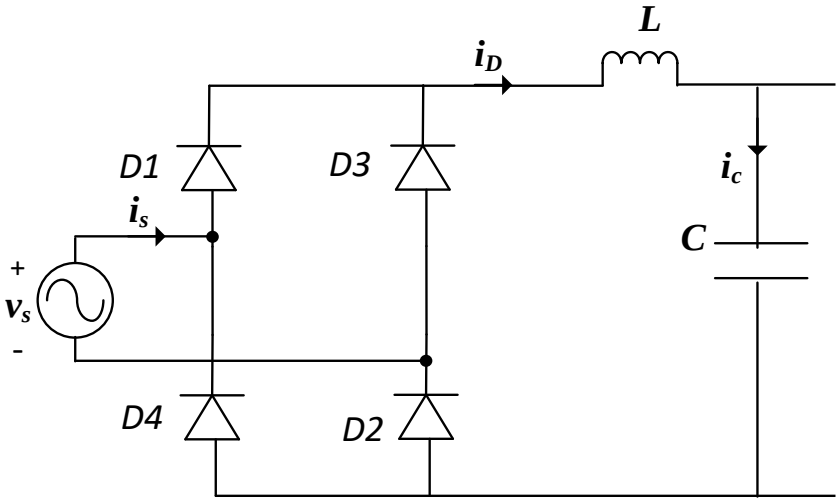
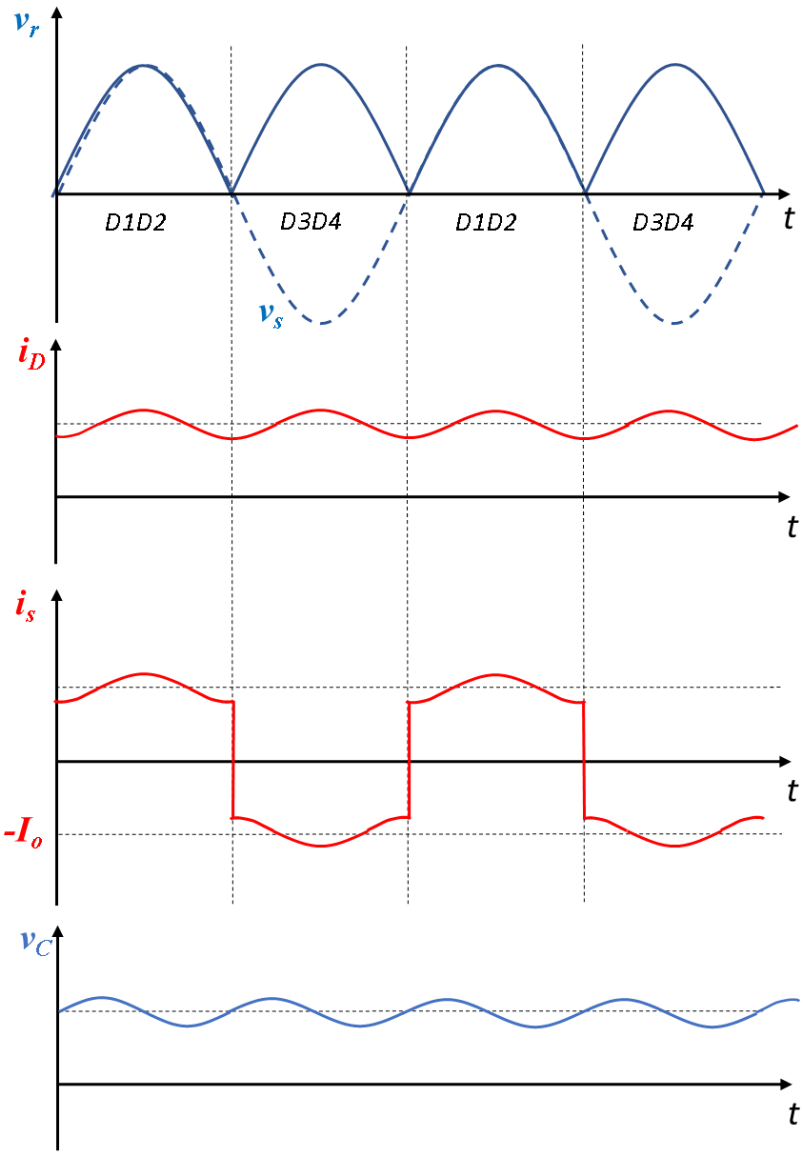
1(f)





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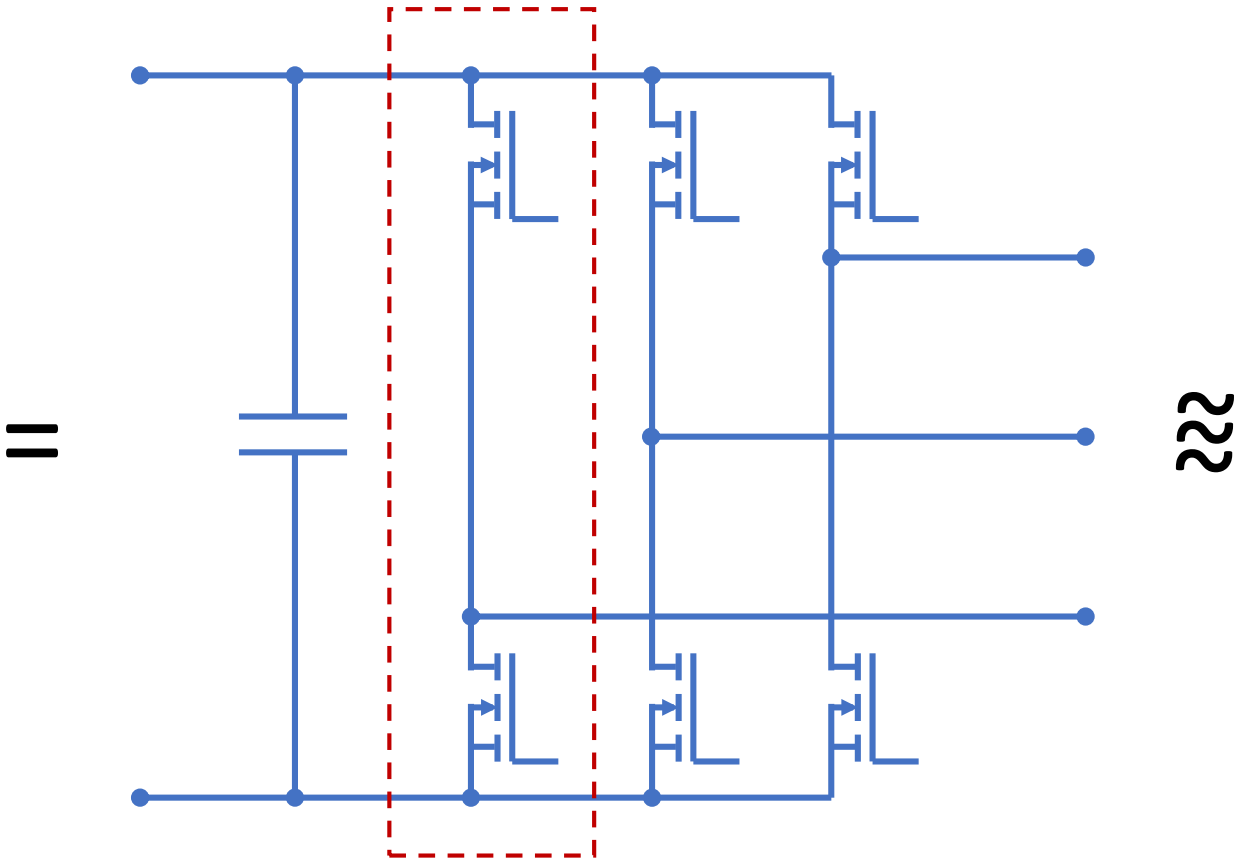
2(a)



Half bridge of two transistors in series

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2(b)

(i) For high efficiency, power electronic circuits avoid operating transistors in the (variable) resistance range but switch them between their most and least conductive modes. Similarly, bridge circuits consisting of two transistors are not operated as in linear circuits as a push-pull stage but either switched fully to the positive or negative supply. That appears to provide two levels per leg/phase as the output versus ground (or another constant potential).
Many loads, such as motors, primarily use the differential output from one leg/phase to another, also called differential mode. Since two (or all) legs/phases can be in the high (or low) level at the same time, the differential voltage can have a third level, 0 V, in addition to positive and negative supply voltage.
To generate any intermediate output voltages, pulse-width modulation presents the available voltage levels sequentially for a limited duration for each so that the output forms the average. Standard pulse-width modulation uses a regular clock or switching rate.

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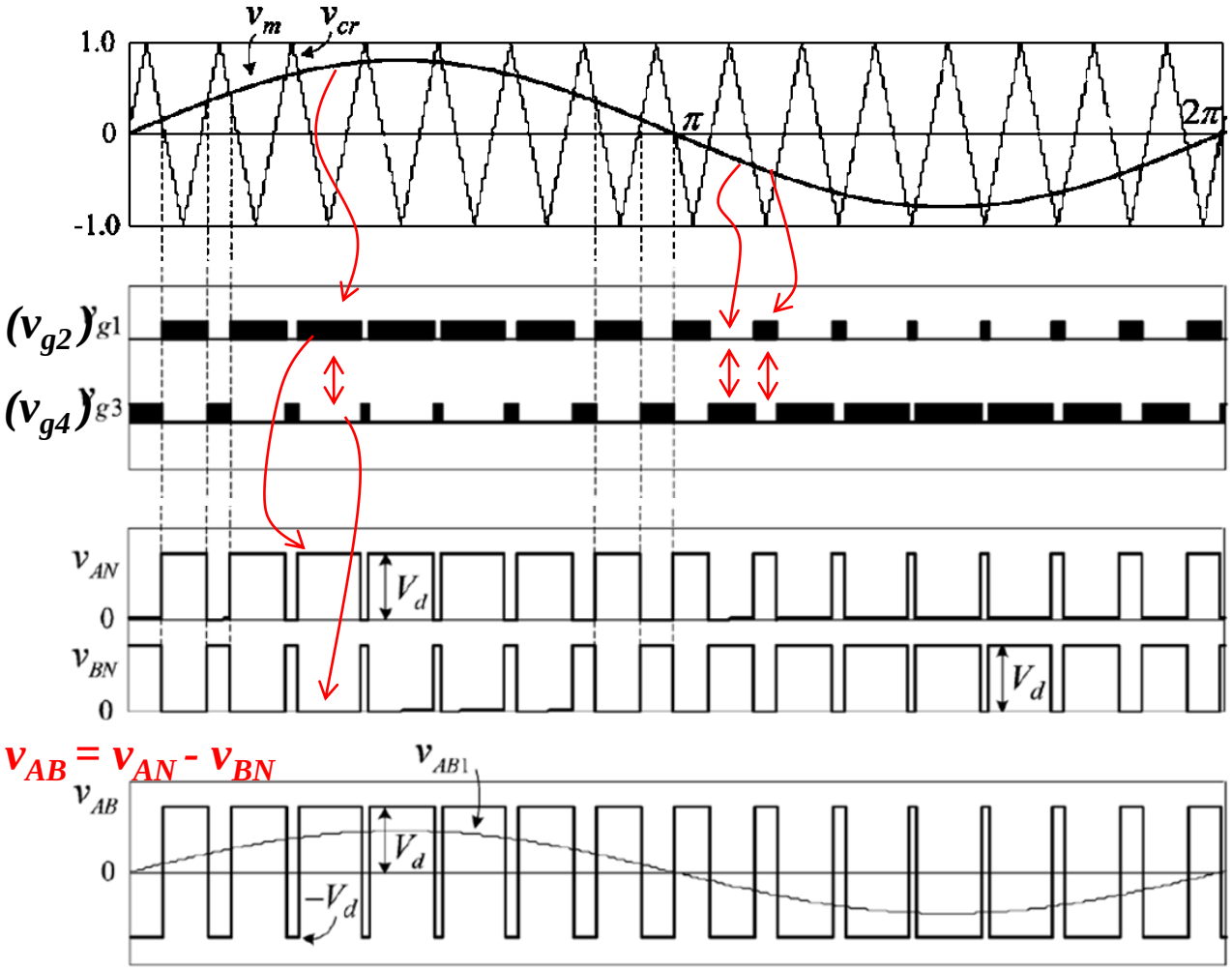
2(b)



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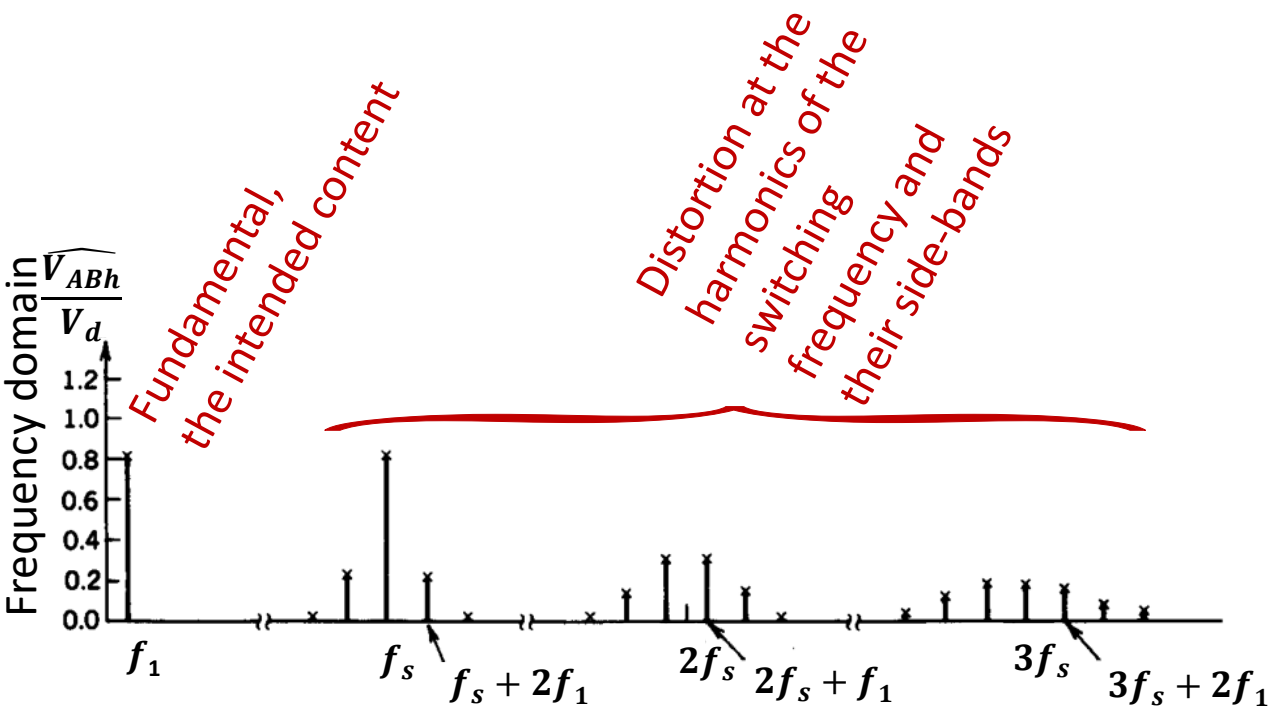
2(b)



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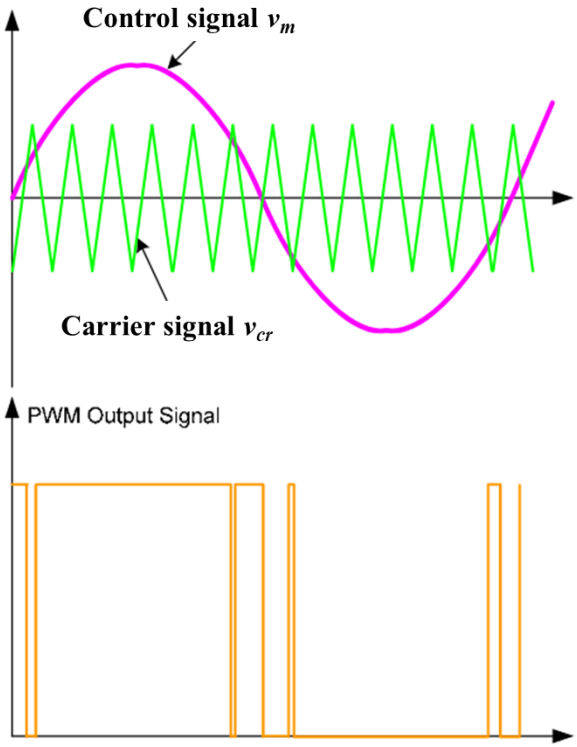
2(b)

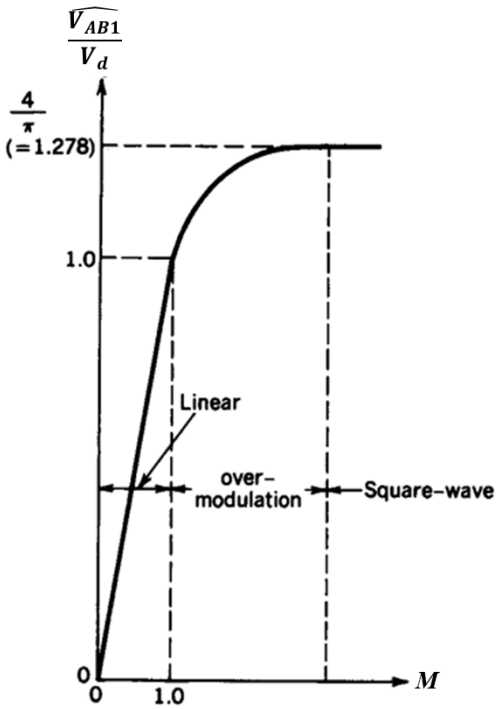
(iii) As in the buck converter, the instant output voltage of an inverter linearly depends on the duty ratio. Thus, the amplitude of the ac output voltage is proportional to the modulation depth and the available dc voltage per

$$v_{AB1} = MV_d \sin 2\pi f_1$$

$$M = \frac{\widehat{V_{AB1}}}{V_d}$$

This relationship only applies until the apex of the sine hits the supply. The output amplitude can in principle be increased further. This regime is called over-modulation. The disadvantage is that the distortion increases. The absolute maximum is at π/4, which is the equivalent sinusoidal content of a rectangular voltage with the available dc voltage.





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2(b)

(iv) The output of a three-phase inverter does in the differential mode not contain any third harmonic of the fundamental (or multiples of it). The reason is that for a three-phase system with 120° phase shift between the phases, the fundamental signals might be different between the phases, but the third harmonic of each phase turns out to be the same signal with the very same phase so that their difference, i.e., the phase-to-phase measurement is 0. The third harmonic does not show up in the differential mode but can certainly be present (or be intentionally injected) in the common mode.
(Optional: In addition to the third and multiples, the second of the fundamental only shows up if there are +/- asymmetries in the generation of the output.)

2(b)

(v) Injecting the same third harmonic of the fundamental into each phase allows increasing the effective differential-mode output amplitude of the voltage for the very same dc voltage as this third harmonic can be aligned such that it subtracts with its own maxima part of the sine maxima of every phase. A third harmonic of the fundamental frequency has by design the same phase relationship with every phase. This injected third harmonic gets eliminated in the differential mode as described earlier.
The easiest is adding a sine with three times the frequency and zero phase. However, also triangular signals work.

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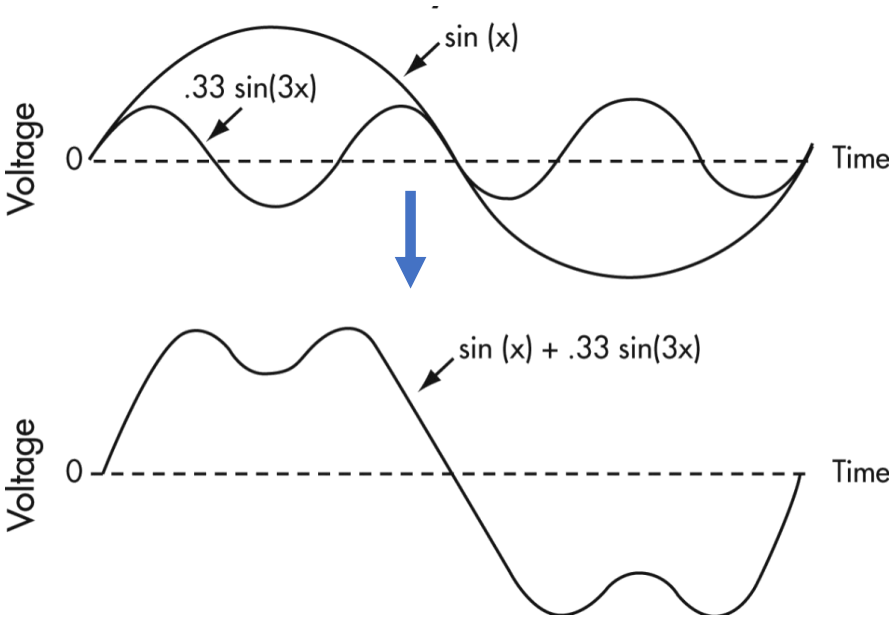
2(b)



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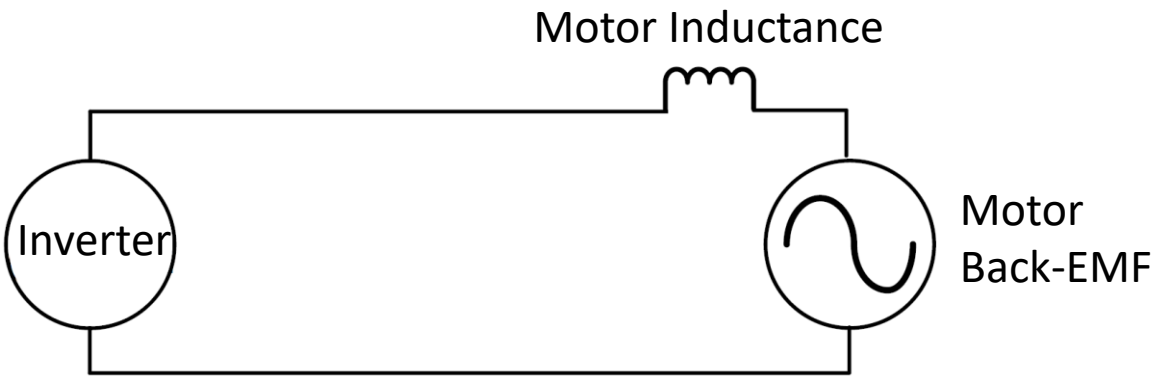
2(c)

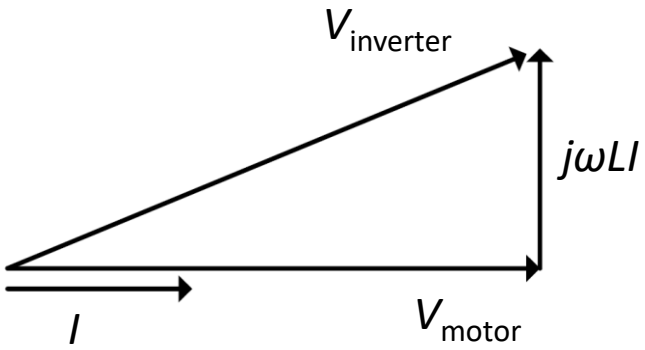
(i) 500 µH phase-neutral; 10 A ripple

$$\frac{V}{\Delta I} = 2\pi f_{\mathrm{sw}} L$$

$$f = \frac{V}{2\pi\ \Delta I\ L} = \frac{800\ \mathrm{V}}{2\pi\ 10\ \mathrm{A}\ \ 500\ \mu\mathrm{H}} = 25.5\ \mathrm{kHz}$$

(ii)





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2(c)

(ii)

$$V_{\text{inverter}}^2 = (\omega L I)^2 + V_{\text{motor}}^2$$
$$= (2\pi \cdot 200\ \text{Hz} \cdot 500\ \mu\text{H} \cdot 10\ \text{A})^2 + (400\ \text{V})^2$$
$$= (400.0493\ \text{V})^2$$

$$\Rightarrow M = \frac{\sqrt{2} \cdot 400.0493\ \text{V}}{800\ \text{V}} = 0.7072$$

Reactance influence small at this frequency so that motor back-emf mostly determines the required modulation depth.

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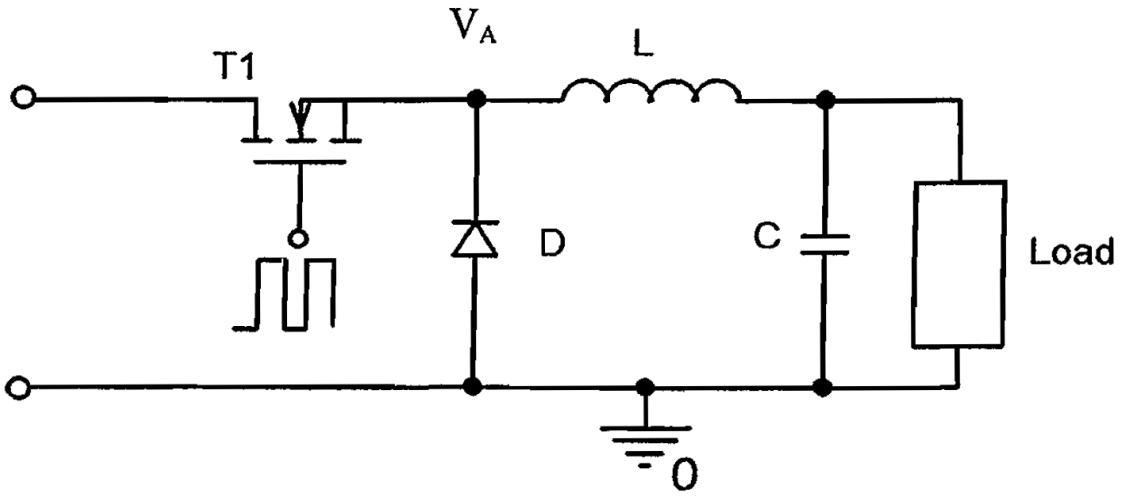
3(a)



3(b)

Buck converters can operate in the continuous and the discontinuous conduction mode. In the discontinuous conduction mode, the inductor is fully demagnetised in every switching cycle and the output current falls to 0. In the continuous conduction mode, the magnetisation and the output current (for the buck converter, both are linearly related for a wide range) just fluctuate a bit around the desired average load current.
The discontinuous mode allows smaller currents with small inductors and low switching frequency. However, for sensitive electronics, smoother operation should be preferred.

3(c)

D from 0.8/3 = 0.267 to 1.2/3 = 0.4 without significant load/losses with 100 A load (keep in mind I_{min} = 0 still as the TPU does not need constantly 50 A):

$$D_{\min} = \frac{0.8\ \mathrm{V} + 0\ \mathrm{V}}{3\ \mathrm{V}} = 0.267$$

$$D_{\max} = \frac{1.2\ \mathrm{V} + R_i I_{\min}}{3\ \mathrm{V}} = 0.533$$

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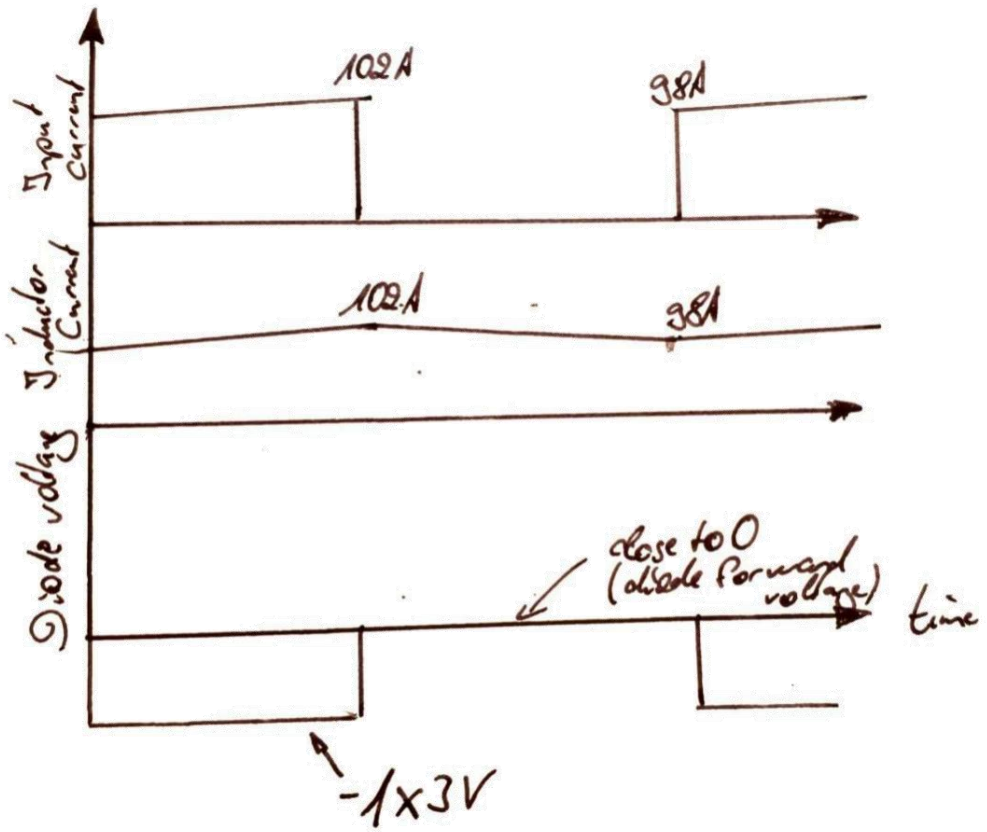
3(d)

$$V = L \cdot \frac{\mathrm{d}I}{\mathrm{d}t}$$

$$1\ \mathrm{V} = L \cdot \Delta I \cdot \frac{f_{\mathrm{sw}}}{2}$$

$$\Delta I = \frac{2 \cdot 1\ \mathrm{V}}{100\ \mathrm{nH} \cdot 5\ \mathrm{MHz}} = 4\ \mathrm{A}$$

3(e)



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3(f)

Diodes have two major problems in power electronics:
They have a non-zero forward voltage (~0.7 V for silicon pn) and can store substantial charge in their pn junction, which can lead to reverse recovery when the diode should turn off after large current flow.

If replaced by Schottky diodes with smaller forward voltage, their typically higher leakage (depends on voltage range) and often less steep current-voltage curve are a compromise.

The diode can be replaced by a transistor that switches every time an ideal diode would conduct. Whereas more parallel diodes do not reduce the problem, the resistance of the transistor switch can be reduced in principle to any level by adding more devices (other disadvantages would certainly lead to a trade-off, though). The saved power would be 50% x 0.7 V x I_{out}

Improvement:

$$-\frac{< loss\ reduction >}{< input\ power >} = -\frac{D \cdot V_{\mathrm{d,fwd}} \cdot I_{\mathrm{output}}}{V_{\mathrm{supply}} I_{\mathrm{output}}}$$

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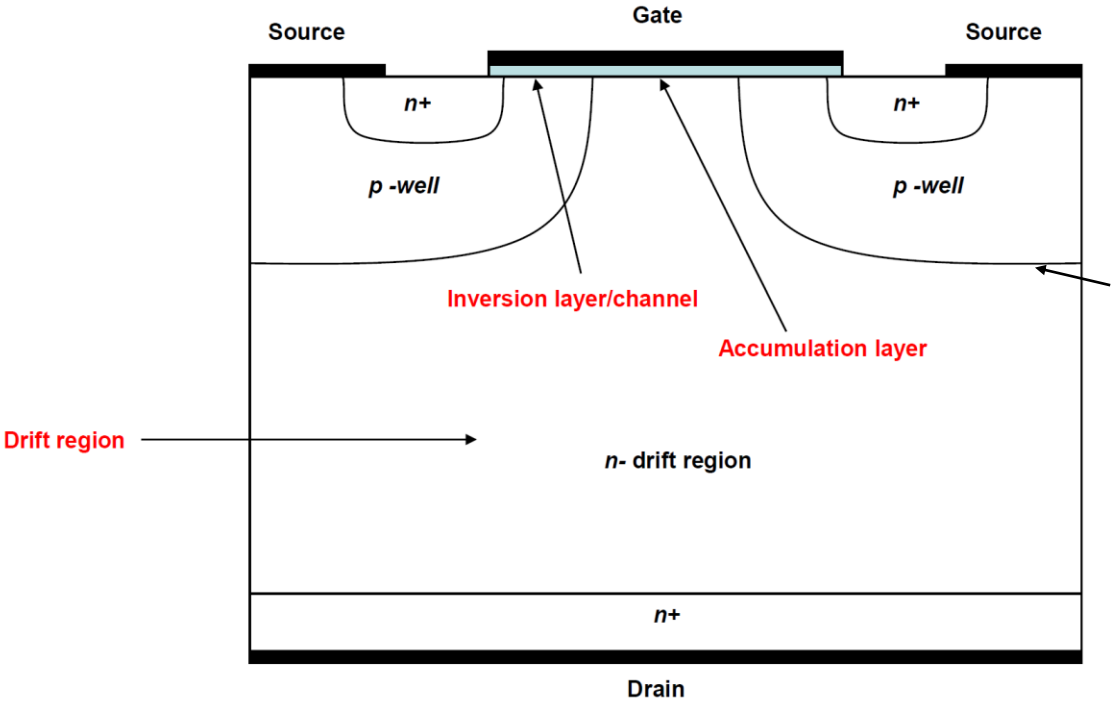
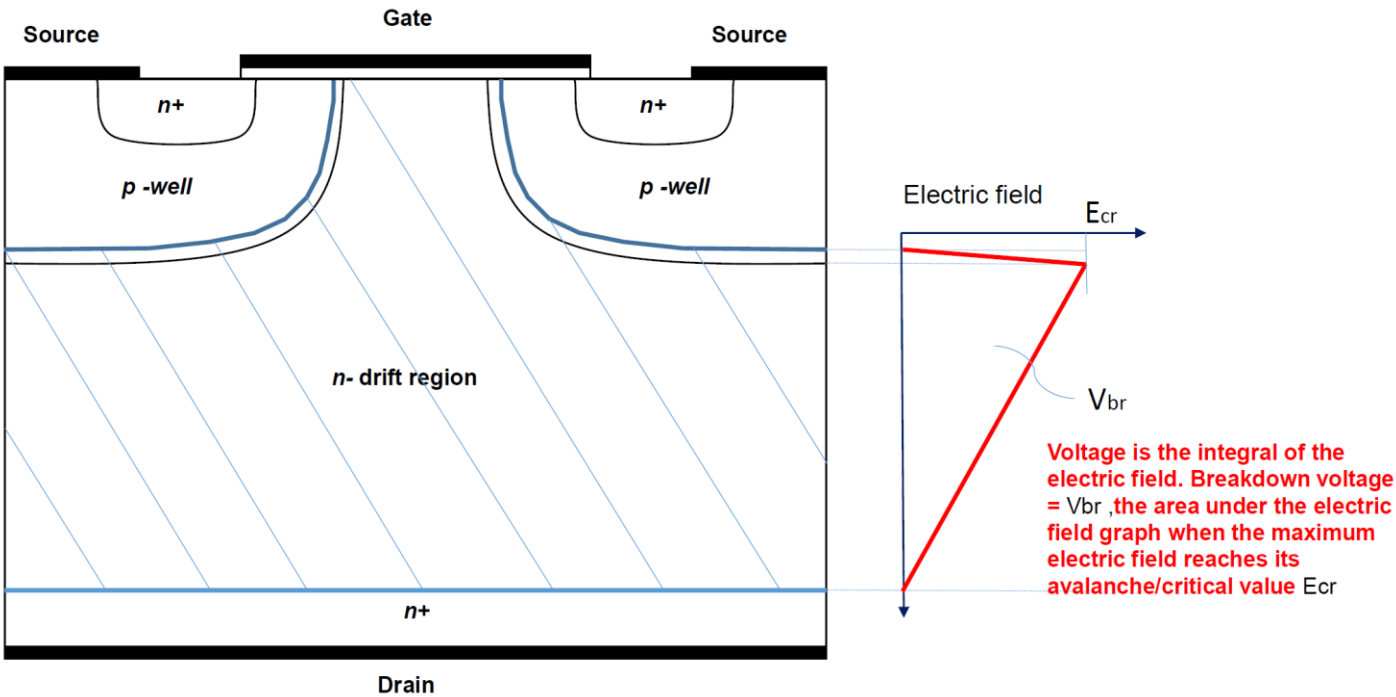
4(a)





3B3, 2024 Lent

4(b)

If such vertical power MOSFETs are designed for higher voltages, their drift region has to grow and absorb the extra voltage (integral over the triangular electric field) without the peak of the electric field reaching the material's break-down strength (or coming even close to it). Though needed in the off mode, the low doping of the drift region however leads to a substantial resistance during conduction so that for higher voltages the drift region is responsible for the majority of the on resistance of the device.

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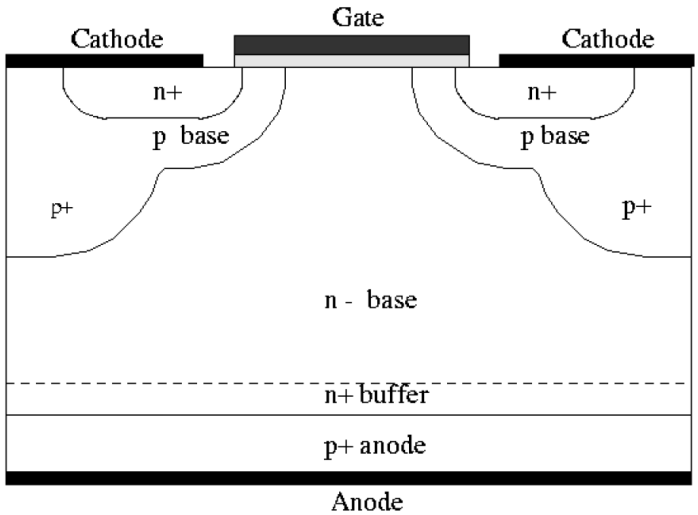
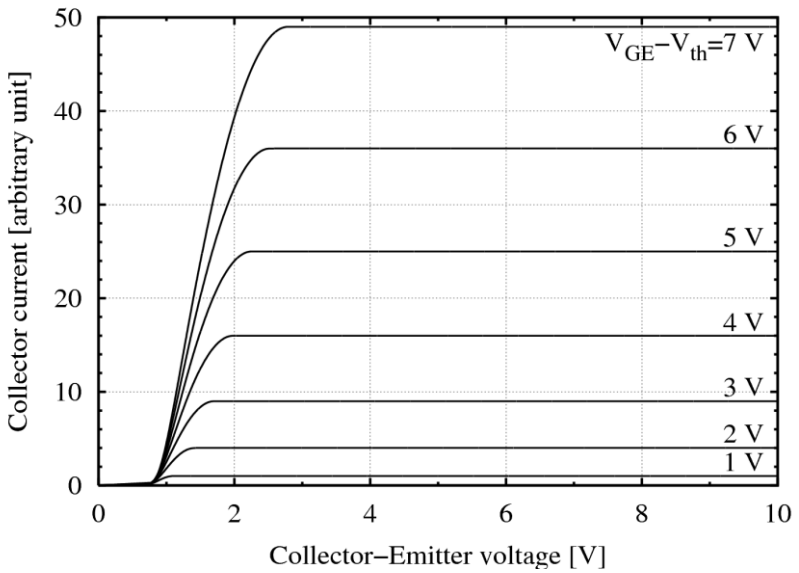
4(c)

Two important differences enable IGBTs:
1. Counter-doping the anode/collector/previous drain so that the end of the n-drift region to form a pn junction.
2. A deep p-region (highly doped) below the cathode/emitter contacts.



The additional pn junction, which is forward-biased for positive collector-emitter voltage, is visible in several ways: curves do not go linearly through 0, but an additional pn voltage (0.7 V or more) have to be overcome before current flows in forward direction. Furthermore, IGBTs without any additional anti-parallel diode do not conduct in the reverse direction (blocking pn junction).



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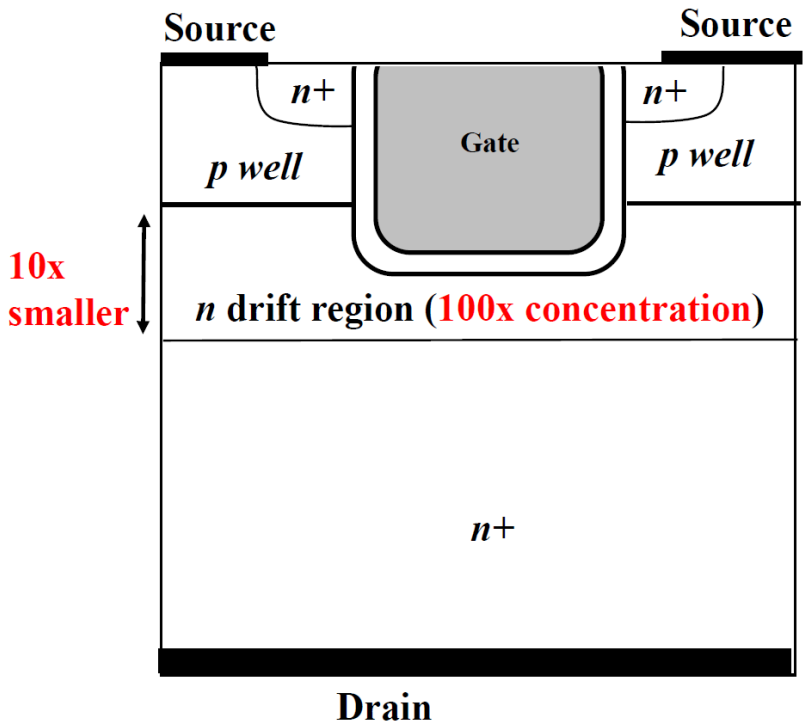
4(d)

The available wide-bandgap materials have a substantially higher bandgap (~factor of three) than silicon, which also requires higher energy levels to damage the materials (ionise etc.). Thus, the break-down field mentioned in 4(b) increases (approximately squared relationship with bandgap) and allows a shorter drift zone for the same or higher operation voltages.

4(d)



The lower carrier mobility would increase the resistance, particularly of the channel, which in the conventional design cannot simply be widened that easily. Therefore, the gate forms a trench to allow for a higher gate density.

Q1 Isolated DC Converter—This was a very popular question with 38 attempts out of 39 students, i.e., all but one student. The mean was 69 out of 100. Part (a) started with sketching the circuits of a rectifier and a fly-back converter as the potentially simplest isolated DC converter. The individual parts were intensively discussed in the lecture, and the question gave some hints how to combine them. Accordingly, most students achieved this part very well and rather left out elements. A typical mistake was ignoring that power transistors (typically in contrast to logic transistors) are not symmetric, i.e., inverting the polarity of transistors or not drawing the symbol fully that the polarity (drain and source) would be identifiable. Part (b) asked for the derivation of the duty cycle, which was demonstrated in the course but also achievable with the techniques repetitively discussed in the lecture for various circuits. Similarly, the traces of fluxes and currents in part (c) were shown and discussed in the lecture but could also be derived using the learnt techniques. Accordingly, these two parts were solved very well by the majority of students. Part (d) asked for some understanding of why operation between the two modes is advantageous. Whereas many students solved this question well, some struggled and provided either descriptive or circular statements instead of a reason or clear advantage. Part (e) discussed a problem of such power supplies by guiding students. First, the question asked for sketches of the input and output currents/voltages. Based on these traces, the question asked about the problems, which were discussed in the lecture in detail. A majority of students solved the question well but left out some parts specifically asked by the question or instead sketched other quantities. Some students mixed the circuit up with others and sketched traces that did not fit the circuit. Furthermore, some students forgot to explain the problem. The last part asked for a filter design and corresponding updated traces. As this question was also covered in the lecture, most students could design a filter topology. However, some students again mixed up the corresponding traces with other circuits or did not provide both voltages and currents at the input and output. Overall, students solved the first three parts best and struggled a bit more with the last three.

Q2 Inverter Circuits—This question was picked by 25 candidates out of 39 students. It covered power inverters as used in variable-speed motor drives. The average was 45 out of 100. The low average was particularly caused by a number of candidates, who only answered a few parts of the question and left the rest blank or provided some answers that did not match the circuit. The question started in part (a) with sketching an inverter circuit and identifying the regular structure, which was done well by almost all students. Very few presented circuits, however, had no similarity with an inverter. Part (b) was about pulse-width modulation, starting with the concept and properties. Several students overestimated the numbers of levels the circuit of part (a) could generate (those suggested five levels phase to phase). The source of these answers could not be reconstructed from the lecture notes. Furthermore, this question discussed the properties and function of the third harmonic in a three-phase inverter, which was covered in the lecture. Still, some students struggled with details that the third harmonic does not evolve differentially on the motor side (if the motor has no access to ground or another stable potential) but can be used to increase the effective differential, phase-phase voltage. Part (c) provided a calculation of a switching rate and the duty cycle for a certain load. Overall, the students demonstrated good understanding of the overall concept of the inverter, though some struggled when it came to details, such as the third harmonic or the number of actual levels generated differentially and relative to ground.

Q3 Non-Isolated DC Converter, Buck Converter—Question 3 was attempted by 38 students out of 39, i.e., all but one student, and overall answered well. The average was 68 out of 100. The focus of this question was knowledge and understanding of the circuit of a buck converter and its behaviour, while the last part included some calculations around the behaviour. Most students had no problems with parts (a) and (b), which involved knowledge covered in the lectures. Again, a number of students sketched transistors with the wrong polarity or no polarity at all. The duty ratio of part (c) included the losses, which was done well by most students, though a number of candidates rather subtracted the losses instead of adding them so that the duty cycle with losses even decreased. Furthermore, a share of students did not recognise the statement that the load, a typical variable processing unit, can be also close to 0 (which is even more common for low operating voltages) so that the lower end of the duty cycle has to consider the case without any load, which is lower as for the loaded case, while the upper end is the duty cycle for maximum output voltage with loss. The switching rate in part (d) was again solved well. Part (e) studied traces across important elements. Although most students solved this question without issues, some mixed it up with other circuits or assumed ideal diodes without suggestion of the question to do so or recognizing that the conditions do not allow for that, which also the subsequent question should have indicated. Part (d) discussed the issues of diodes in such fast-switching and low-voltage circuits. Although most candidates understood this issue, some missed the point and provided unrelated diode properties.

Q4 Device Technology—Question 4 focussed on device technology and transistor structures. Although overall solved by most students very well, only 20 out of 39 students, thus, approximately half of them, picked the question. The average was 60 points out of 100. Parts (a) and (b) covered the vertical power field-effect transistor and specifically for knowledge covered identically in the course. Accordingly, most students performed very well. A typical problem was mixing up doping

or not indicating elements in very rough sketches. Some candidates appeared to not have fully understood the issue of field-effect transistors at high voltages and how IGBTs solve that. Part (b) served as a bridge to part (c), which was likewise solved well overall but with gaps here and there or dopings mixed up. Some students did not include all typical features in the sketch. Again, some sketches were rough and without any legend. Furthermore, some students missed the second sub-part asking concretely for features. Part (d) was knowledge, this time about the value of wide-bandgap materials, which are currently growing in importance, and Part (e) about a structure of SiC as one such material. In the last question, a number of students mixed up the typically vertical structure of SiC with planar GaN transistors. Furthermore, several students just repeated the standard MOSFET.