1° (a) $$M = \frac{\hat{V}_{ph}}{V_d/2} = \frac{\hat{V}_{LL}/\sqrt{3}}{V_d/2} = \frac{\sqrt{2}V_{LL}/\sqrt{3}}{V_d/2} = \frac{2\sqrt{6}}{3}\frac{V_{LL}}{V_d}$$

When non-linear modulation, the max phase voltage is a square wave
For the square wave, the fundamental has peak value as $\frac{4}{\pi}$ of the square wave.

$$\hat{V}_{ph} = \frac{4}{\pi}V_{dc}, \quad \hat{V}_{LL} = \frac{4\sqrt{3}}{\pi}V_{dc}, \quad V_{LL} = \frac{2\sqrt{3}}{\pi}V_{dc}$$

(b) When linear modulation: $\hat{V}_{LL} < \frac{\sqrt{3}}{2}V_d$

When non-linear modulation: $\frac{\sqrt{3}V_d}{2} < \hat{V}_{LL} < \frac{2\sqrt{6}}{\pi}V_d$

Non-linear modulation allows larger A.C voltage.

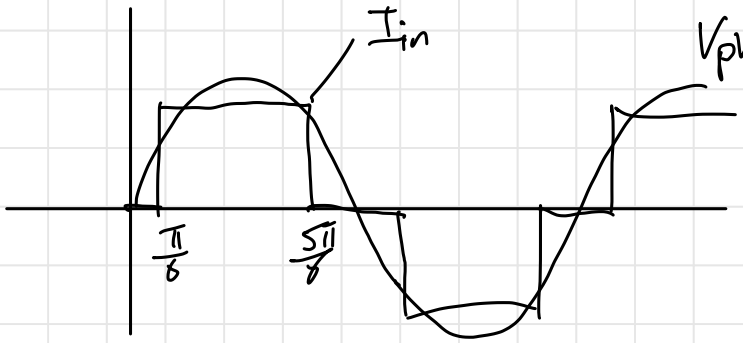
The switching frequency is reduced when non-linear modulation, therefore the switching loss is reduced.

The harmonics are increased by non-linear modulation.

(c) $$V_{dc} = \frac{3}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} \sqrt{2}\times 400\left(\sin 100\pi t + \frac{\pi}{6}\right) d\,100\pi t$$

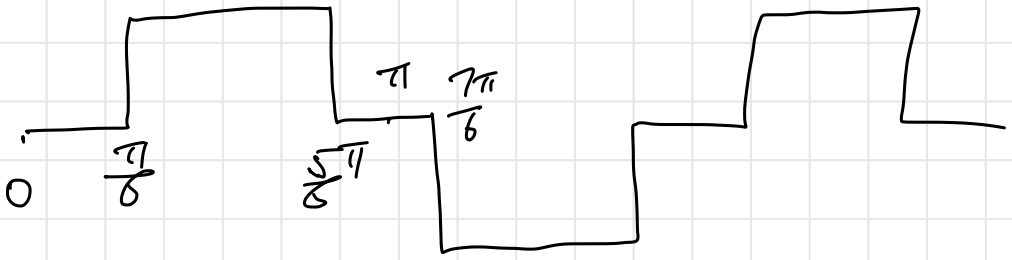
$$= \frac{3}{\pi}\times\sqrt{2}\times 400 = 540\ V.$$

(d)



$$I_{in} = \frac{3\sqrt{2}V_{LL}}{\pi R}$$

(e)



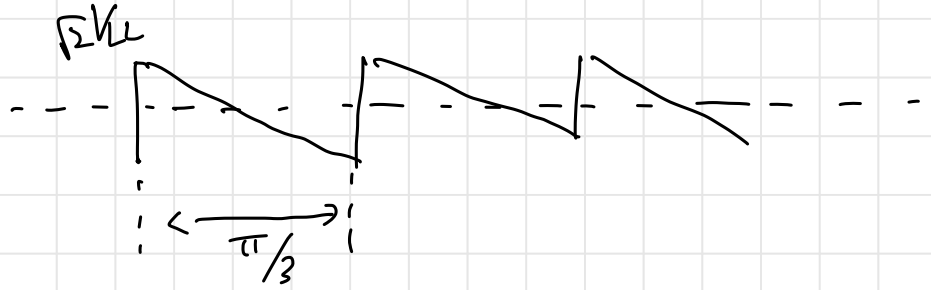
Fourier series of the waveform

$$i_h = \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \frac{2\sqrt{3}}{\pi} \cdot \frac{3\sqrt{2}V_{LL}}{\pi R} \sin(n \cdot 100\pi t)$$

Three phase system has no triplen harmonics.

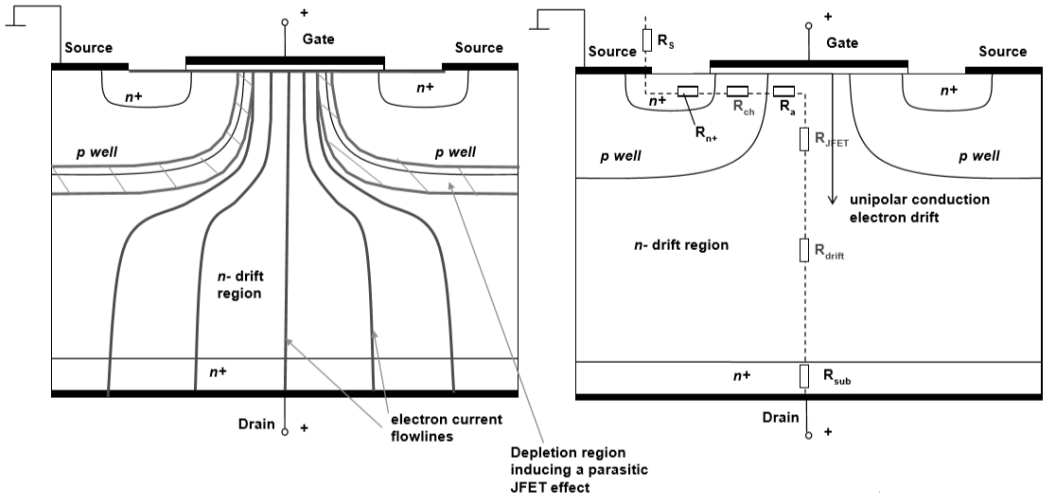
$$I_h = \sum_{n=1,5,7,\ldots}^{\infty} \left(\frac{6\sqrt{6}}{\pi^2 n} \frac{V_{LL}}{R} \right)$$

(f)



The input current will be largely distorted due to large DC capacitor therefore the input current will have large harmonics and the drive will have a poor power factor.

Q2. (a)



The JFET effect is due to the depletion region expansion in the “neck” region of the power MOSFET – that is the region between two adjacent p-wells. This depletion region is due to the reverse bias of the junctions between p-wells and the drift region, when a positive potential is present on the drain with respect to that of the source potential. The JFET depletion region further narrows down the electron current path within the neck region. This is because the electric field created within each of the adjacent depletion regions pushes the electrons away in the space between the depletion regions.

RDS(ON) is made up of the series combination of all the parts of the device between the source and drain where there is a voltage drop due to the electron current flow. Some of these components are negligible in some voltage ranges. Note that we assume to operate in the linear region of operation of the on-state.

RDS(ON) = Rs + Rn+ + Rch + Ra + RJFET + Rdrift + Rsub

• In general the package resistance Rs, the source resistance Rn+ and the silicon substrate resistance Rsub, are negligible, but their effect in low-voltage, high current devices can still be significant.

• The channel resistance Rch and the accumulation layer resistance Ra, play an important role, especially for the low-voltage devices.

The Rdrift is the drift region resistance which is closely determined by the breakdown voltage of the device

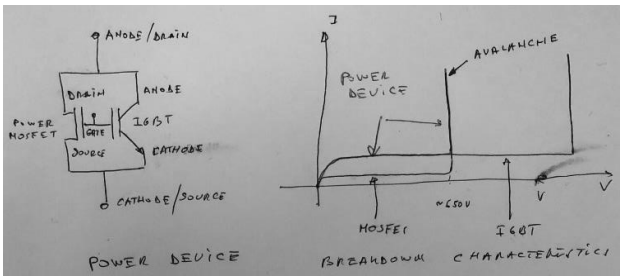
(b) The specific drift resistance is governed by the doping and the thickness of the drift region. Because the critical electric field is 10x higher in SiC than in Si, the doping concentration in the drift region and the thickness of the drift region of a SiC Power MOSFETs can be up to 100x higher and respectively 10x smaller than that in Silicon. Taking into account that the mobility of carriers in Silicon is about 2x of that of carriers in SiC, the specific drift resistance can be ~500X smaller in Sic when compared to Si. This is a very significant advantage, especially for higher classes of voltage ratings (e.g. above 600 V), where the drift region resistance is the most important component of the total on-state resistance.

The JFET resistance is also smaller in SiC, as the extension of adjacent depletion regions associated with the p-well/n-drift region junction is smaller. This is because of the higher doping of the n- drift region in SiC when compared to Si..

The channel and accumulation specific resistances are however higher in SiC than in Si because of the low channel mobility in SiC (30-100x smaller than in Silicon). The channel and accumulation layer resistances tend to be important at lower voltage ratings (e.g. below 600 V), where SiC power MOSFETs have less or no advantages compared to Si Power MOSFETs.

The other resistances play a minor role at higher voltages (e.g. above 600V) where SiC is considered as substitute to Silicon.

(c) (i)

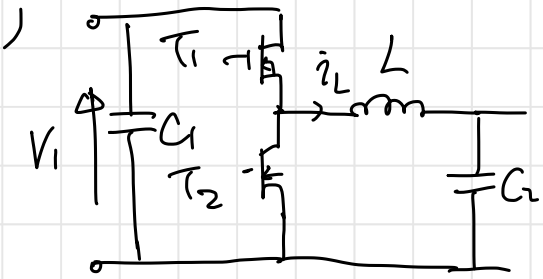


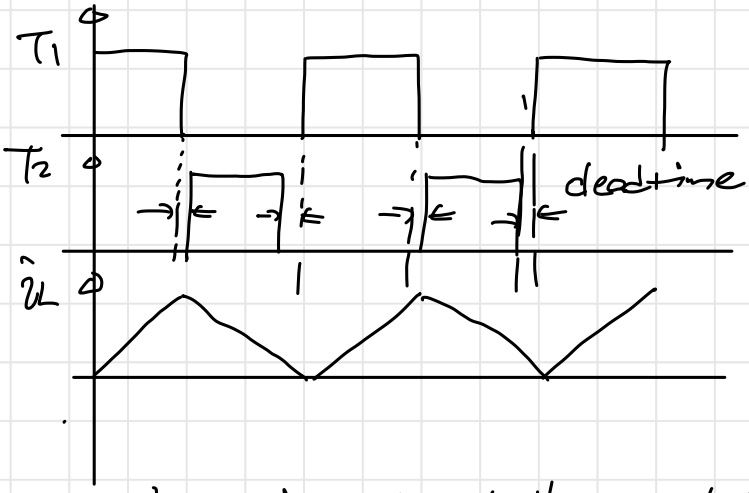
The devices are connected in parallel. Since the MOSFET has a lower voltage rating, the breakdown (which is ~ the rated voltage + a 10% margin) will be dictated by the MOSFET. The MOSFET device will be first to enter the avalanche regime. In other words the power device, combining the two devices will be limited by the breakdown of the MOSFET (see picture). In terms of the leakage, given that the two devices have the same surface area, the IGBT leakage will be significantly larger than the MOSFET leakage. This is because the leakage is amplified by the bipolar action of the pnp transistor that exists in the IGBT. Therefore the device will have mostly the leakage of the IGBT and the avalanche breakdown of the MOSFET [20%]

(ii) During the reverse conducting mode, only the MOSFET will conduct through its intrinsic PIN diode (also known as the anti-parallel diode). The internal PIN diode in the MOSFET is formed between the p well (as the anode of the PIN diode), the n- drift region (as the intrinsic region of the PIN diode) and the n+ drain (as the cathode of the PIN diode). No reverse conduction can occur in through the IGBT, as the open-base PNP transistor will block the current during the reverse mode operation. Note that there is no anti-parallel diode present in the IGBT [20%]

Q3. (a)

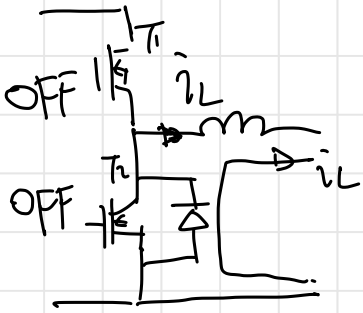
(i)





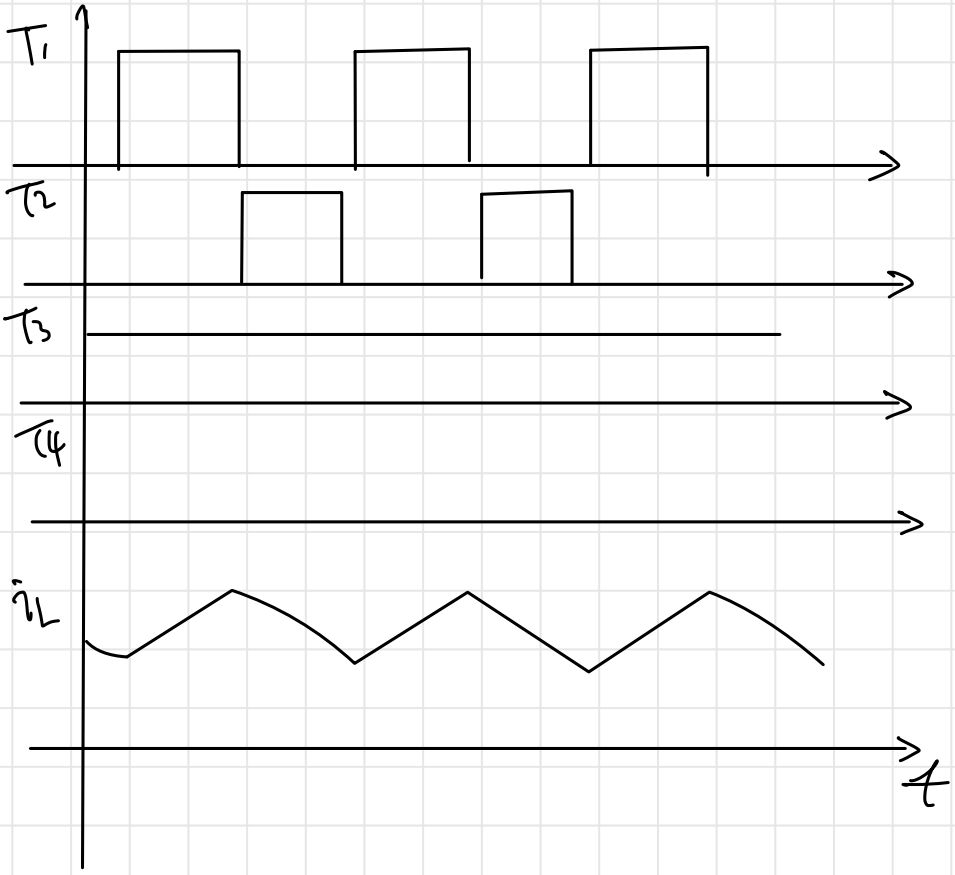
The deadtime is used to avoid T_1 and T_2 being incidently switched on at the same time. Both T_1 and T_2 are switched off at the same time for a short interval of time.

(ii)



During the deadtime, T_2 is off but i_L needs to be continuous. T_2 as a MOSFET contains a body diode which conduct this commutating current i_L from the source to the drain of T_2. This commutating current results in near zero voltage of T_2, therefore, T_2 will be switched on (after this deadtime) at nearly zero voltage. The switching loss of T_2 is thus reduced.

(b) (i) T_3 keeps on. T_4 keeps off. T_1 and T_2 are complementary switching at switching frequency. Duty cycle is D, switching period is T. $(\frac{1}{T} = f)$



When T_1 is on, T_2 is off, $\Delta i_L = \frac{V_i - V_o}{L} DT$

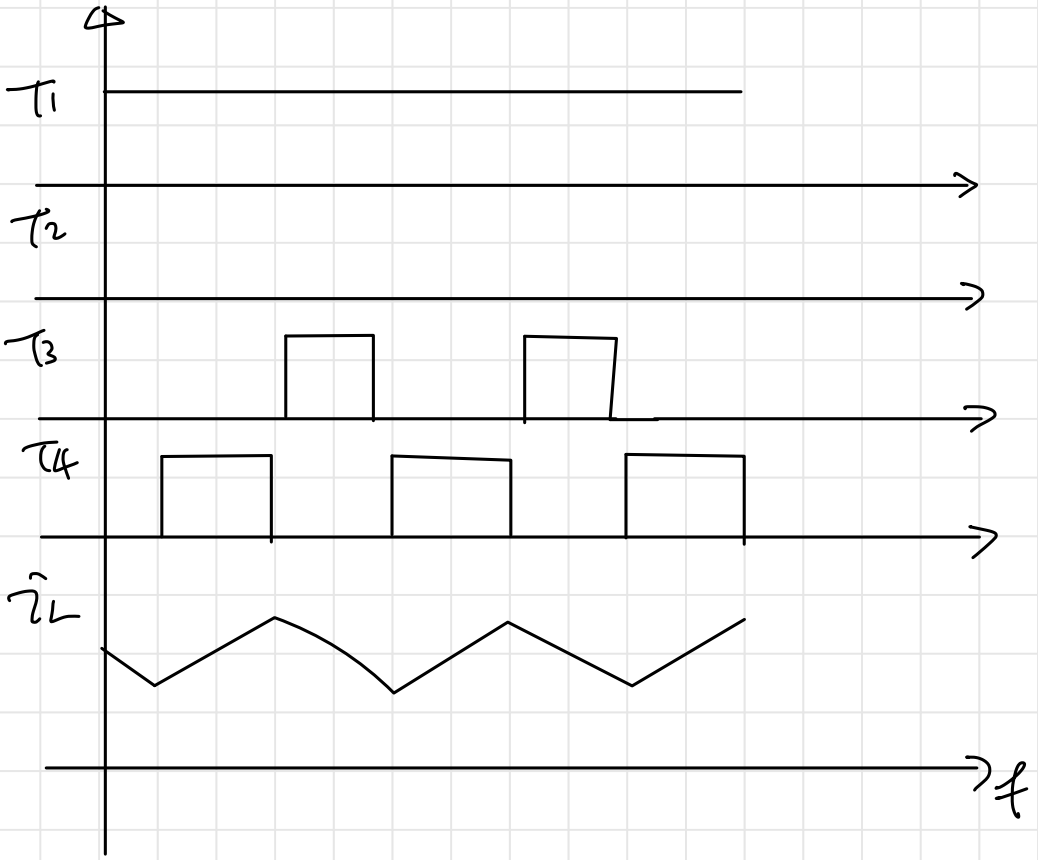
When T_2 is on, T_1 is off $\Delta i_L = \frac{V_o}{L}(1-D)T$

Continous current. $(\frac{V_i - V_o}{L})DT = \frac{V_o}{L}(1-D)T$

$$\frac{V_o}{V_i} = D$$

(ii) T_1 and T_4 switch together, T_2 and T_3 switch together.

T_1 (T_4) switch complementary to T_2 (T_3).



When T_1, T_4 are on: $\Delta i = \frac{V_i}{L} DT$

When T_2, T_3 are on: $\Delta i = \frac{V_o - V_i}{L} (1-D)T$

Continous current of inductor.

$$\frac{V_i}{L} DT = \frac{V_o - V_i}{L} (1-D)T$$

$$\frac{V_o}{V_i} = \frac{1}{1-D}$$

Q4. (a) (i) $V_2 = \frac{N_2}{N_1} \frac{D}{(1-D)} V_1$

When switched on, $V_1 = \frac{\Delta i_s}{DT} L_m$, $\Delta i_s L_m = V_1 DT$

$\Delta \phi \cdot N_1 = \Delta i_s L_m = V_1 DT$.

When switched off, $\Delta \phi \cdot N_2 = \frac{\Delta i_d}{(1-D)T} \cdot \frac{L_m}{N_1^2/N_2^2} = V_2 (1-D) T$

$\frac{V_1 DT}{N_1} = \frac{V_2 (1-D) T}{N_2}$, $\frac{V_2}{V_1} = \frac{N_2}{N_1} \frac{D}{(1-D)}$

Continous flux: $N_1 V_1 DT = N_2 V_2 (1-D) T$

$$\frac{V_2}{V_1} = \left(\frac{D}{1-D}\right) \frac{N_2}{N_1}$$

(ii) the minimum L_m is when critical conduction of flux in the transformer core, i.e. no offset of flux. Due to lossless system.

$I_1 V_1 = I_2 V_2$, $I_1 = \frac{40 \times 10}{400} = 1A$

When critical conduction of flux the input current is also in critical condention.

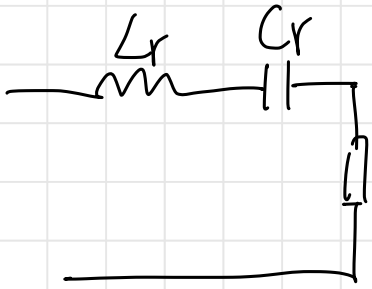
Therefore, for DT, the average input current I_1 is half of the peak current in DT, $I_{1pk} = 4A$

$$L_m = \frac{V_i DT}{I_{pk}} = \frac{400 \times 0.3 \times \frac{1}{100 \times 10^3}}{4} = 500\mu H.$$

The minimum L_m is $500\mu H$.

(b) (i) $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$, $\omega_r = \frac{1}{\sqrt{L_r C_r}}$

(ii) $L_m \gg L_r$. LLC is approximately LC.



$$R_T = \left(\frac{N_2}{N_1}\right)^2 \frac{8R}{\pi^2}.$$

$$V_o = \left|\frac{R_T}{R_T + Z_r}\right| \cdot V_{ac} = \frac{1}{2}\left|\frac{R_T}{R_T + Z_r}\right| V_i$$

$$Z_r = \frac{j\omega L_r \cdot \frac{1}{j\omega C_r}}{j\omega L_r + \frac{1}{j\omega C_r}} = \frac{\frac{L_r}{C_r}}{\frac{1 - \omega^2 L_r C_r}{j\omega C_r}} = \frac{j\omega L_r}{1 - \omega^2 L_r C_r} = \frac{j\omega L_r}{1 - \omega^2/\omega_r^2}$$

$$\left|\frac{R_T}{R_T + Z_r}\right| = \left|\frac{R_T}{R_T + \frac{jwL_r}{1-(w/w_r)^2}}\right|$$

$$= \left|\frac{1}{1 + \frac{jwL_r/R_T}{1-(\frac{w}{w_r})^2}}\right| \quad \text{if } \frac{wL_r}{R_T} = Q$$

$$= \left|\frac{1}{1 + \frac{jQ}{1-(\frac{w}{w_r})^2}}\right| = \frac{1}{\sqrt{1 + \frac{Q^2}{\frac{(1-w^2)^2}{w_r^2}}}}$$

if $\frac{w}{w_r} = w_n$

$$= \frac{1}{\sqrt{1 + Q^2\left(\frac{1}{w_n} - w_n\right)^2}} \qquad \text{Gain} = \frac{1}{\Sigma} \frac{1}{\sqrt{1 + Q^2\left(\frac{1}{w_n} - w_n\right)^2}}$$

$$Q = \frac{wL_r}{R_T}, \qquad R_T = \frac{N_2^2}{N_1^2}\frac{8R}{\pi^2}$$

(iii)