1 (a) (i) The usual simplified expression for the ripple voltage ΔV assuming instantaneous charging and discharge over a whole half cycle is

$$\Delta V = \frac{I}{2fC}$$

where f is the supply frequency, C is the smoothing capacitance and I the load current.

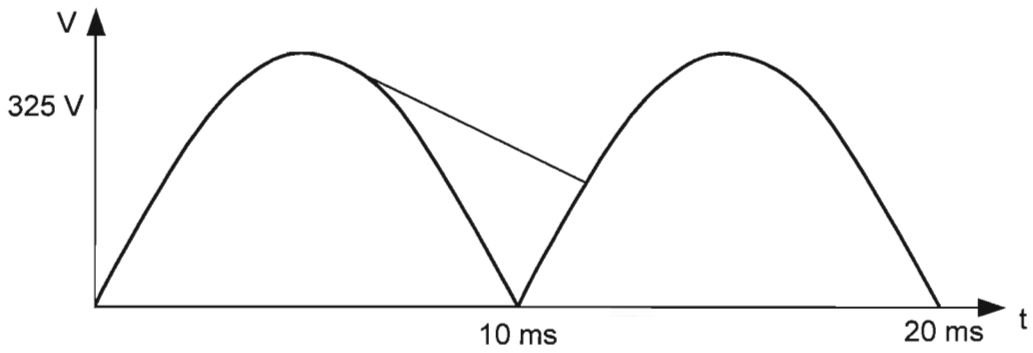
[5%]

(ii) First find the current – assume this is constant on the basis that the voltage ripple is small.

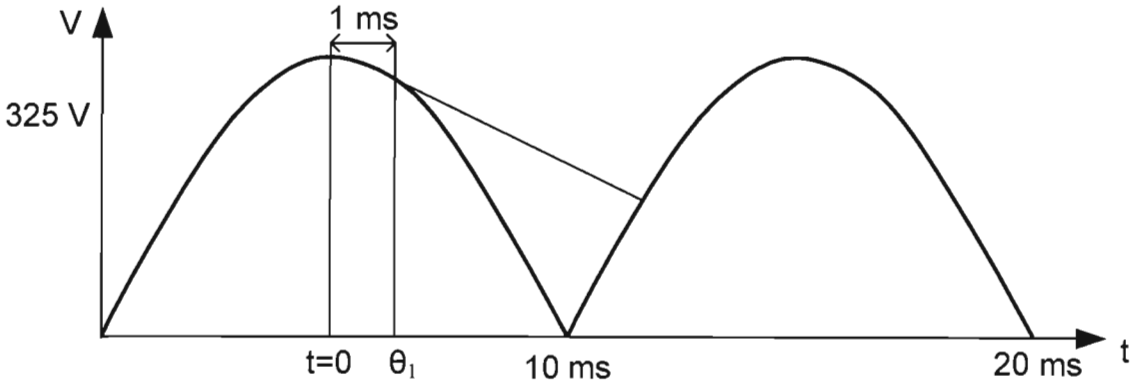
$$I = \frac{230\sqrt{2}}{2300} = 0.14 \text{ A}$$

Hence the ripple is 298 V. [5%]

(iii) The approximation that the ripple is small i.e. that the RC time constant is long compared to the half period of the mains waveform is unjustified, as indicated on the sketch. [15%]



(iv) A proper calculation involves a decaying capacitor voltage, starting some time after the peak of the sine wave, meeting a rising sine wave. The start of the discharge is when the capacitor's discharge current is approximately 0.14 A.



$$I_c = C\frac{d}{dt}(325\cos\omega t)$$

$= -325\omega C \sin \omega t$

$\omega t = 16.9°$ **or 0.296 radians**

$\therefore t_d = 0.94ms \quad (\sim 1ms)$

At this point the voltage is 325 cos 16.9 = 311 V. So the decay is

$311e^{-\left(\frac{t-t_D}{\tau}\right)}$ hence $\tau = RC - 10.8$ ms

The next half sine wave starts to rise 5 ms after the peak of the previous half sine wave. Voltage is $-V\cos\omega t$ with $t = 0$ at peak of previous half sine wave.

Time (ms)	Decaying voltage	Rising voltage
7 ms	177	191
6.8 ms	181	174
6.87 ms	180	180

Intersection is after 6.87 ms. Diode conduction starts at 6.87 ms, continuing for 0.94 ms after the peak at 10 ms. Overall conduction time is therefore 4.07 ms (out of 10 ms).

Ripple current is $\frac{325}{2300} - \frac{180}{2300} = 63$ mA peak to peak [35%]

(v) As the conduction times of the diodes are relatively long, the mains side current is not too peaky. Also, a small capacitor is small and cheap. Any ripple at this frequency in the current and hence light output may be tolerable. [10%]

(b) (i) With a smoothing capacitor, up to delay angles of 90°, it would always be charged fully to the peak of the incoming mains voltage. Control would only be possible for longer delay angles, so0 a good control characteristic would not be possible. [5%]

(ii) The average (mean) voltage from the combination of triac and bridge rectifier (without a smoothing capacitor) is given by integrating the voltage over a half cycle.

$V_{MEAN} = \int_{\alpha}^{\pi} \sqrt{2V} \sin \omega t \, d\omega t$

$= \frac{\sqrt{2V}}{\pi}(1 + \cos\alpha)$

where α is the angle of delay. Maximum output is at $\alpha = 0$ and is 10% when

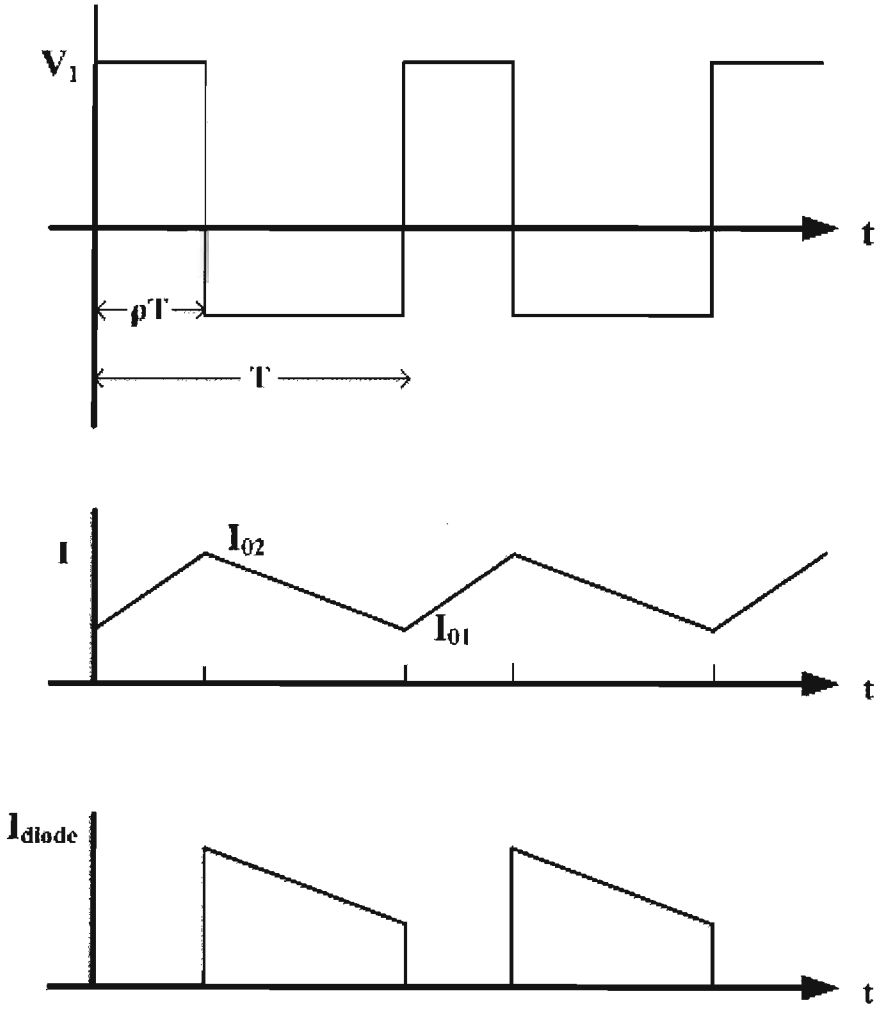
$(1 + \cos\alpha) = 0.2$

i.e. α 143° [15%]

(iii) A linear regulator from the output of the bridge to a low voltage such as 14 V will have high losses and one of the selling points of LED lamps is their energy efficiency! As a nearly constant voltage is needed across the LEDs, say about 14 V for eight in series, it is easy to add an extra winding to the transformer of the fly back converter feeding the LEDs to give a convenient auxiliary power supply. [10%]

2(a) It is a simple single-transistor circuit and the circuit is appropriate for the power level of interest (say about 100 W). It is a low cost circuit. It also, importantly, provides galvanic isolations between the input (mains connected) side and the output – an essential safety feature. [10%]

(b) Waveforms of the primary voltage, the current in L_O and the secondary diode current.



[25%]

(c) During current build up in L_O, the applied voltage is V_{DC} and the transformer secondary is open. I_n integral from:

$$I_{O1} - I_{O2} = \frac{1}{L_O}\int_o^{\rho T} V_{DC}\,dt$$

$$= \frac{1}{L_O} V_{DC}\,\rho T$$

where I_{O2} and I_{01} are magnetizing inductance currents and ρ is the duty cycle of the switch. When the transistor is off the primary voltage is a reflection of the secondary which is at V_O.

$$I_{O1} - I_{O2} = \frac{1}{L_O}\int_{\rho T}^{T} \left(-\frac{N_1}{N_2} V_O\right) dt$$

$$= -\frac{N_1}{N_2}\frac{V_O}{L_O}(1-\rho)T$$

Equating the changes in current and rearranging gives

$$V_O = V_{DC}\frac{N_2}{N_1}\left(\frac{\rho}{1-\rho}\right) \qquad [20\%]$$

(d) (i) At the highest input voltage, the duty cycle should be at a minimum. Try $\rho = 0.2$

$$\frac{N_2}{N_1} = \frac{V_O}{V_{DC}}\left(\frac{1-\rho}{\rho}\right) = 18:1$$

At the lowest input voltage, the duty cycle should be at a maximum. Try $\rho = 0.8$

$$\frac{N_2}{N_1} = 112:1$$

At 140 V in, and 18:1 ratio, gives ρ as

$$\rho = \frac{1}{1+\frac{N_2}{N_1}\frac{V_{DC}}{V_O}} = 0.39$$

At 360 V in and 112:1 ratio

$\rho = 0.61$

So ranges are $\rho = 0.61$ to 0.8 for 112:1, and $\rho = 0.2$ to 0.39 for 18:1. Many options for the turns ratio exist – about 50:1 would be a compromise. [25%]

(ii) For a given amount of converted power, the RMS value of primary or secondary currents increases at extreme values of duty cycle. With a small duty cycle, the stress is on the primary side and for large values of duty cycle the stress is on the secondary. In the first case the losses rise in the transistor and transformer primary; in the second case in the transformer secondary and ultimately in the diode.

(iii) When the transistor is off, it must withstand V_{DC} plus the reflected secondary voltage, i.e. $V_O \, {}^{N_1}\!/_{N_2}$

So, if $N_1 : N_2$ is 50:1, and the maximum value of $V_{DC} = 360$ V, then the transistor must stand at least

360+250 = 610 V

It would be wise to allow for overshoots etc.

N.B. expressing the transistor voltage as $V_{DC} + {}^{N_1}\!/_{N_2} V_O$ and using the relationship between V_{DC} and V_O gives $V_{DC}\left(\frac{1}{1-\rho}\right)$

indicating that using shorter duty cycles reduces the stress on the switch. [10%]

3 (a) (i) One of the standard modulation schemes can be used. One of the 'modern' schemes such as space vector modulation has the advantage of better utilization of the DC link and relatively easy digital implementation. The important point is that the switching frequency should be high enough to be inaudible, i.e. above 18 kHz. [10%]

(ii) For this application, again any standard modulation scheme can be used with a preference for space vector modulation. The switching frequency can be 5 to 10 kHz as the drive is being used in an industrial setting and this frequency range ensures relatively low losses. [10%]

(iii) The main point in terms of modulation scheme is that fixed ratios of modulating to switching frequency will be used, with so-called 'gear changing' i.e. step changes in this ratio as the train speed varies. [10%]

(b) (i) For example, consider the line voltage $V_{AB} = V_A - V_B$

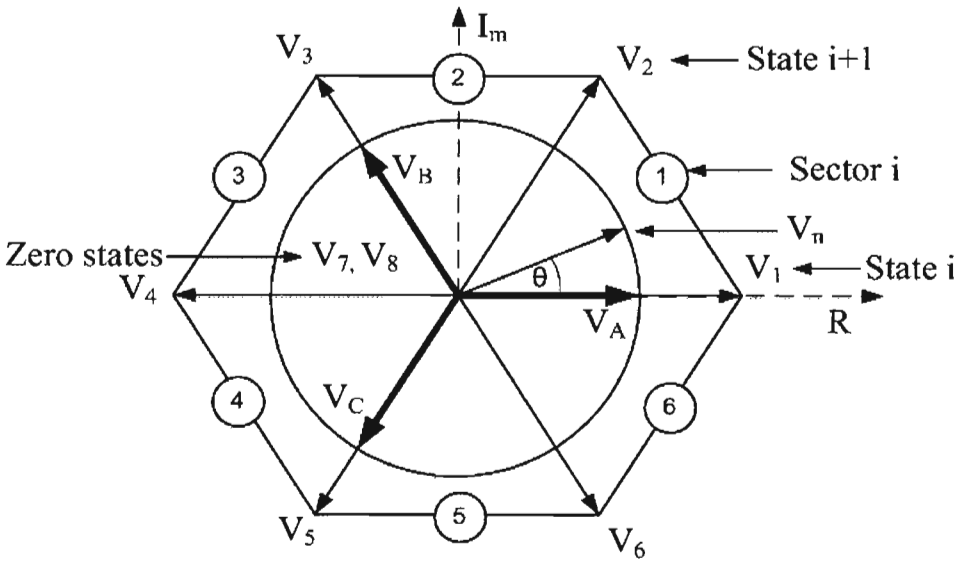
State	V_A	V_B	V_C	V_{AB}
V_1	1	0	0	1
V_2	1	1	0	0
V_3	0	1	0	-1
V_4	0	1	1	-1
V_5	0	0	1	0
V_6	1	0	1	1
V_7	1	1	1	0
V_8	0	0	0	0

The magnitude of V_{AB} can be controlled by the use of the zero states V_7 and V_8. In practice, it is better to use pairs of vectors, e.g. V_1 and V_2, and the zero states to get nearer to a pure sinewave ouput, e.g.

V_8 V_1 V_2 V_7 V_7 V_2 V_1 V_8

[35%]

(ii)

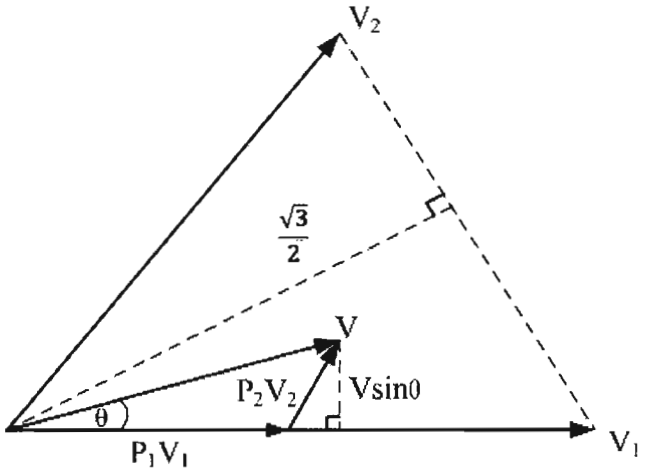


[10%]

(iii) Direct-direct uses particular zero states in particular sectors, namely V_7 in sectors 1, 3 and 5. V_8 is used in the other sectors V_1, V_2, V_7, V_1, V_2, V_7, V_1

Direct-inverse uses both zero states in each sector, reducing the number of switching events V_1, V_2, V_7, V_2, V_1, V_8, V_1 [10%]

(iv)



Duty cycles are ρ_1 and ρ_2

$$\rho_2|V_2|\cos 30 = V\sin\theta$$

$$= m\hat{V}\sin\theta$$

Also $\hat{V} = \frac{\sqrt{3}}{2}|V_2$

So $\rho_2|V_2|\frac{\sqrt{3}}{2} = m\frac{\sqrt{3}}{2}|V|\sin\theta$

Or $\rho_2 = m\sin\theta$

[15%]

4 (a) (i) Unipolar devices such as the MOSFET have an on-state characteristic which is essentially resistive, in the case of a MOSFET described as R_{DSON} . The resistance of the channel is augmented by the drift region resistance in the case of higher voltage MOSFETs. Super junction devices enable the on-state resistance to be reduced. In contrast, there is high level carrier injection in the IGBT leading to conductivity modulation in the drift region. The on-state characteristic shows that significant current flows only above about ~0.7 V and then a resistive characteristic develops. The differences make MOSFETs more suited to low voltage applications and IGBTs more suited to high voltage, high current applications. [10%]

(ii) The MOSFET's switching losses are relatively low as there is no stored charge to remove from the channel though device capacitances need to be charged and discharged. In the case of the IGBT, it takes time to remove the stored charge from the device so current flows with voltage applied even though the device is nominally off. This tail current is the source of significant loss, usually limiting the operating frequency. [10%]

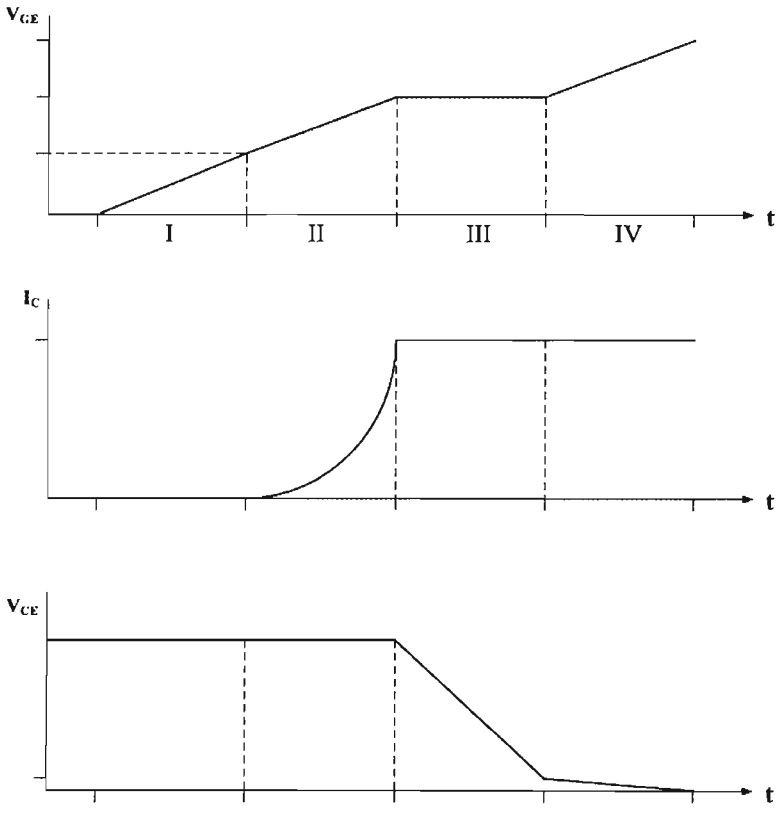
(b) (i) The power and hence currents are low. A part with at least a 400 V breakdown voltage is needed. The switching frequency is modest ~40 kHz. A MOSFET is suitable as switching losses are low and on-state losses will be low too as the current is small. The bipolar transistor is an alternative, and may well be cheaper. [10%]

(ii) The DC link voltage will be around 560 V and the currents substantial (nearly 30A). This is IGBT territory. A moderate switching frequency (say 10 kHz) is acceptable both from performance and IGBT loss perspectives. [10%]

(iii) The relatively high switching speed points towards MOSFETs. The voltages are low so devices with very low on-state resistances can be used, so both on-state and switching losses will be modest. [10%]

(c) (i) The load is inductive in character and so can be regarded as a constant current over the switching period. The clamping refers to the use of a free wheel diode to transfer the load current to the DC supply when the switch is off. An ideal diode clamps the maximum voltage seen by the switch to the value of the DC supply. [10%]

(ii)



[20%]

(iii) During the fall of drain voltage the gate voltage remains constant, having reached a value such that the drain current is 20 A

So $V_{GE} = \sqrt{\frac{20}{2.5}} + 6 = 8.83$ V

The current into the gate from the gate driver balances the current through the reverse transfer capacitance

$$\frac{12 - 8.83}{R_G} = 50.10^{-12} \frac{dV_{DS}}{dt}$$

The drain voltage is to fall 300 V in 50 ns

Sp $\frac{dV_{DS}}{dt} = 6$ V/ns

Hence $R_G = 10.6\ \Omega$ (10 is nearest preferred value).

(iv) The voltage at gate before the start of the fall of drain voltage is $V_{GE} = 12\left(1 - e^{-t/T}\right)$

Where $T = R_G \times C_{iss} = 16$ ns

$t = 21.3$ ns [20%]