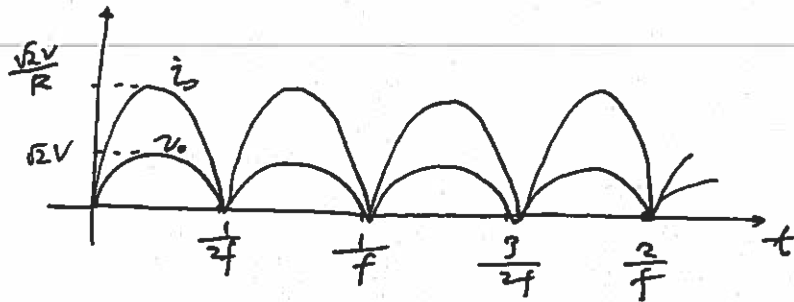
3B3 2020 Cribs

Q1

(a)



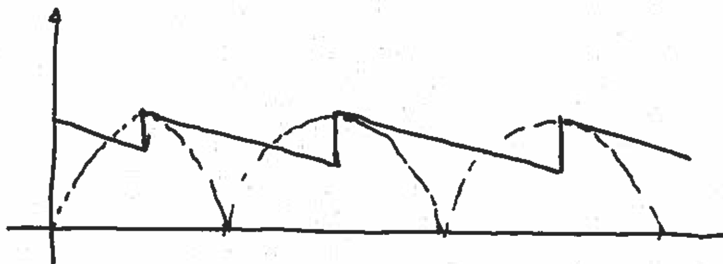
$$V_o = \frac{1}{\pi}\int_0^{\pi} \sqrt{2}V\sin 2\pi f t = \frac{2\sqrt{2}}{\pi}V$$

$$I_o = \frac{V_o}{R} = \frac{2\sqrt{2}V}{\pi R}$$

$$v_o(\omega t) = \frac{2\sqrt{2}V}{\pi} - \frac{4\sqrt{2}V}{\pi}\sum_{n=2,4,6\ldots}\left(\frac{1}{n^2-1}\cos n\omega t\right)$$

when $n=2$, $$V_{o2pk} = \frac{2\sqrt{2}V}{\pi} + \frac{4\sqrt{2}V}{3\pi} = \frac{10\sqrt{2}}{3\pi}V$$

(b)

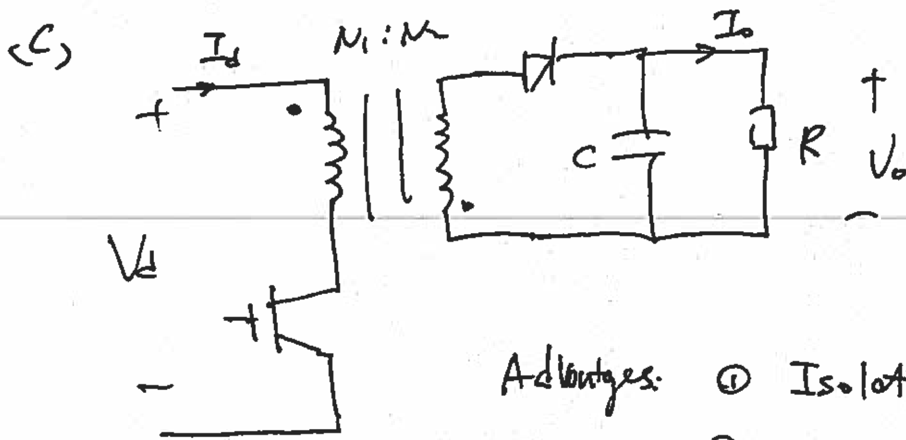


$$\Delta V_o = \sqrt{2}V - \sqrt{2}V\left(1 - \frac{1}{2fRC}\right) = \frac{\sqrt{2}V}{2fRC}$$

Assumptions: ① Linear discharge of capacitor C, $RC \gg \frac{\pi}{2\pi f}$

② The discharge takes over the half cycle, i.e. the charge-up is effectively instantaneous.

(c)



Advantages: ① Isolation between input and output

② Same voltage polarity of input and output, can be grounded at both sides.

(d) $P_o = 50W$

$$V_o = \frac{P_o}{I_o} = \frac{50}{10} = 5V.$$

$$\frac{V_o}{V_d} = \frac{N_2}{N_1} \frac{D}{1-D} \quad , \quad \frac{N_2}{N_1} = \frac{1-D}{D} \cdot \frac{V_o}{V_d}$$

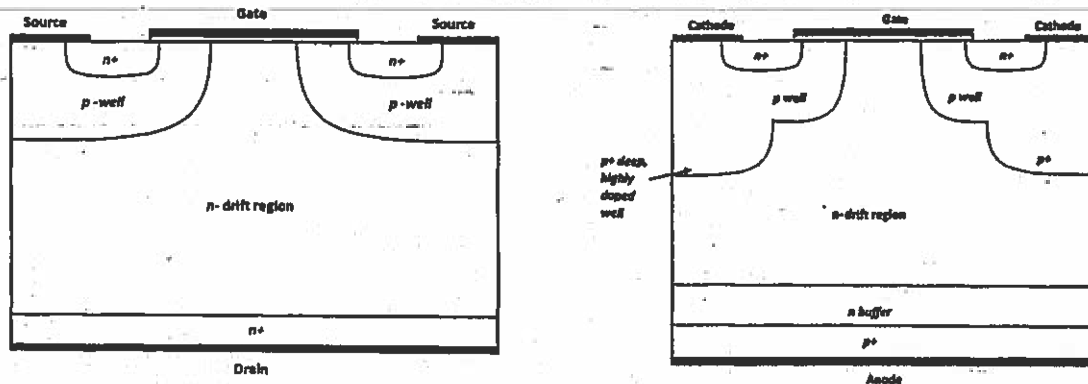
If neglecting voltage ripples. $V_d = \sqrt{2}V = 230 \cdot \sqrt{2}$

$$\frac{N_2}{N_1} = \frac{1-0.4}{0.4} \cdot \frac{5}{230 \cdot \sqrt{2}} = \frac{3}{92 \cdot \sqrt{2}} = 0.02305$$

$$\approx \frac{23}{1000} \text{ or } \frac{3}{130}$$

Answers

(a), The cross-section structures of the MOSFET (left picture) and IGBT (right picture) are shown below:



The top parts of the MOSFET and IGBTs are very similar featuring an n+ Source/Cathode and a MOS channel formed at the surface of the p-well and controlled via the gate terminal placed on top of an insulated gate region. The MOS channel connects the n+ Source/Cathode to the top of the n- drift region. At the bottom part of the drift region the IGBT has a P+ hole injector. This injector becomes the emitter of a pnp transistor and the anode of the internal PIN diode leading to conductivity modulation. The conductivity modulation could result in an increase in the conductivity of the drift region by one to two order of magnitude. As a result the on-state performance of the IGBT is in general better than that of the MOSFET. However this is at the expense of higher switching losses in the IGBT, as the plasma needs to be formed during the turn-on and removed during the turn-off

(b). The saturation in the MOSFET refers to current saturation and is due to the pinch-off of the MOS channel at high drain voltages. The saturation in a bipolar transistors refers to voltage saturation as the minimum voltage drop between the emitter and collector when the base current is increased, In the bipolar saturation both the emitter-base and collector base junctions are forward biased.

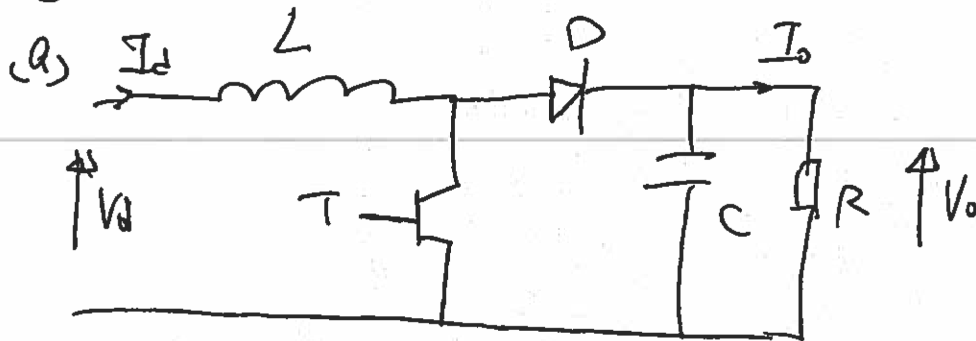
There are three important regions in the on-state:

- Active region. In this case the base-emitter junction is forward-biased while the base-collector junction is reverse-biased.
- The quasi-saturation is the condition where the stored charge (plasma) moves into the collector region reducing significantly the depletion region and eventually removing it completely. In this regime, the base-collector junction becomes forward-biased.
- The saturation occurs when the whole collector region is filled with plasma (excess mobile carriers) and the base-collector junction is fully forward-biased.

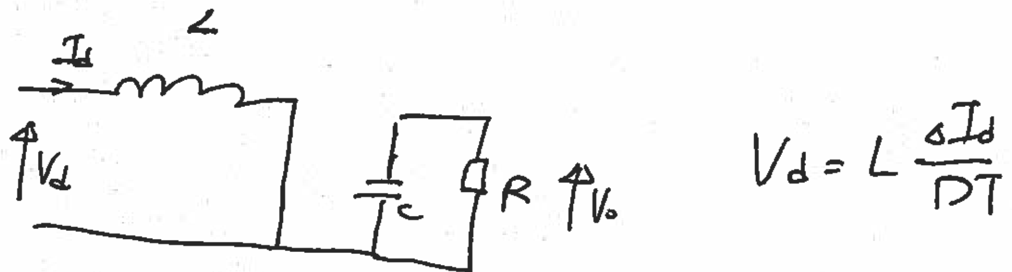
- Deep saturation or hard occurs when additional charge is built in the collector region leading to excess carriers to increase well above the doping even in the proximity of the n+ collector region.

Q3

(a)

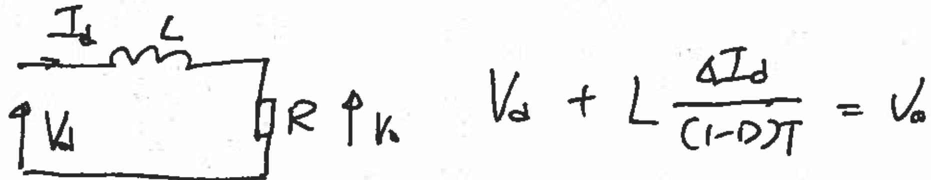


T is ON:



$$V_d = L\frac{\Delta I_d}{DT}$$

T is OFF:



$$V_d + L\frac{\Delta I_d}{(1-D)T} = V_o$$

$$V_d + \frac{L}{(1-D)T}\cdot\frac{V_d \cdot DT}{L} = V_o \Rightarrow V_d + \frac{V_d \cdot D}{1-D} = V_o$$

$$M(D) = \frac{V_o}{V_d} = \frac{1}{1-D}$$

(b) To find the critical current at the inductor to judge inductor current continuity.

The inductor average current is same to the input average current.

$$V_d I_d = \frac{V_o^2}{R}, \quad \frac{V_o}{V_d} = \frac{1}{1-D} \quad \text{when CCM}$$

$$I_d = \frac{V_d}{(1-D)^2 R}$$

If the average inductor current is less than the half of the inductor peak to peak ripple, discontinuous current.

$$\Delta I_{p\text{-}p} = \frac{V_d}{L} \cdot DT_s$$

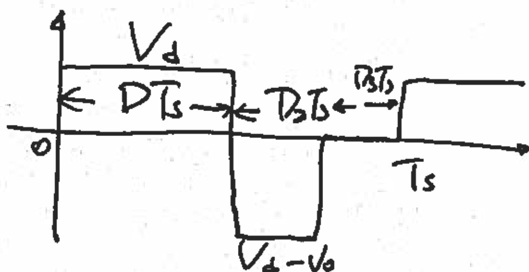
therefore: for DCM. $I_d < \frac{V_d D T_s}{2L}$

$$\frac{2L}{RT_s} < (1-D)^2 D \; , \quad \frac{2L}{RT_s} = k$$

$$k < (1-D)^2 D$$

(c)

Voltage of the inductor:

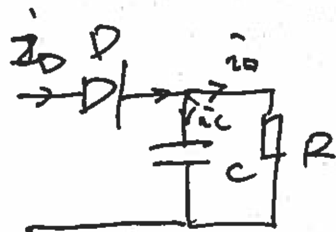


$$\int_0^{T_s} V_L = \int_0^{DT_s} V_d \, dt + \int_{DT_s}^{(D+D_2)T_s} (V_d - V_o) dt + \int 0 \, dt = 0$$

$$DV_d + D_2 (V_d - V_o) = 0$$

$$V_o = V_d \frac{D + D_2}{D_2}$$

Current at the capacitor connecting node. Using KCL



$$\int_0^{T_s} i_D dt = \int_0^{T_s} i_c dt + \int_0^{T_s} i \, dt$$

$$\int_0^{T_s} i_o dt = \frac{V_o}{R} T_s$$

$$\int_0^{T_s} i_D \, dt = \frac{1}{2} \cdot \left(\frac{V_d}{L} DT_s\right) \cdot D_2 T_s \quad \text{(solving area of geometry of } i_D \text{)}$$

$$\frac{V_o}{R} T_s = \frac{V_d D T_s^2 D_2}{2L} \Rightarrow \frac{V_o}{R} = \frac{V_d D D_2 T_s}{2L} \Rightarrow K = \frac{V_d}{V_o} D D_2$$

$$D_2 V_o = V_d D + V_d D_2 \Rightarrow D_2 = \frac{V_d D}{V_o - V_d}$$

Therefore:

$$K = \frac{V_d}{V_o} \cdot \frac{V_d D^2}{V_o - V_d} \Rightarrow V_o^2 - V_o V_d = \frac{V_d^2 D^2}{K}$$

$$\frac{V_o^2}{V_d^2} - \frac{V_o}{V_d} - \frac{D^2}{K} = 0 \qquad \frac{V_o}{V_d} = M$$

$$M^2 - M - \frac{D^2}{K} = 0$$

$$M = \frac{1 + \sqrt{1 + \frac{4D}{K}}}{2}$$

(d) When $D = 0.5$, DCM.

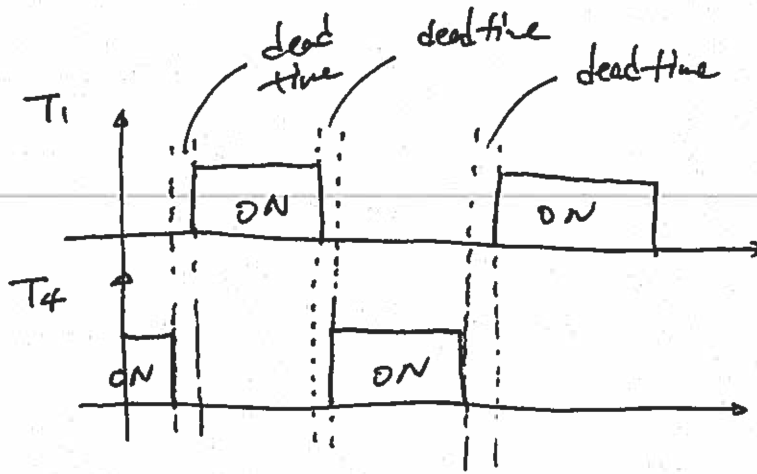
$$\frac{V_o}{V_{in}} = \frac{1 + \sqrt{1 + \frac{4D}{K}}}{2} = \frac{1 + \sqrt{1 + 4 \times 0.5^2 / 0.096}}{2} = 2.181$$

When $D = 0.7$, CCM.

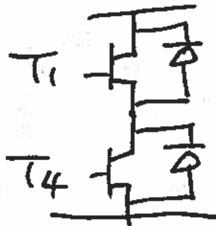
$$\frac{V_o}{V_{in}} = \frac{1}{1-D} = 3.333$$

Q4.

(a)



Two devices connected as a half bridge, top: T_1, bottom: T_4.



T_1 and T_4 are switched complementary and the ideal switching is that two devices change status instantaneously. i.e when one device is turning on the other is turning off at the same time.

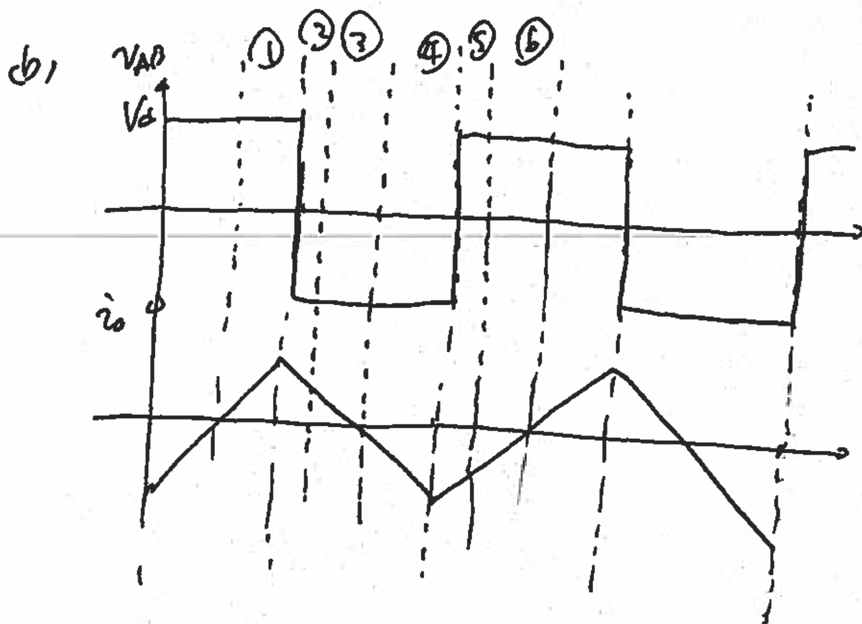
However, due to potential delay of gate drive and tolerance of different devices. instantaneous switching may cause a short moment when both devices are on, which will cause short circuit.

A dead-time is inserted between two devices to ensure the complementary device is off when the device is turning on.

Therefore, a short moment when both devices are off is created.

To implement the dead time, the switching on is slightly delayed.

(b)



①: $T_1 T_2$ ON, current path $T_1 T_2$

②: $T_1 T_2$ OFF, $T_3 T_4$ OFF } → deadtime, current path $D_4 D_3$

③: $T_3 T_4$ ON, current path $D_4 D_3$

④: $T_3 T_4$ ON, current path $T_3 T_4$

⑤: $T_3 T_4$ OFF, $T_1 T_2$ OFF } → dead time, current path $D_1 D_2$

⑥: $T_1 T_2$ ON, current path $D_1 D_2$

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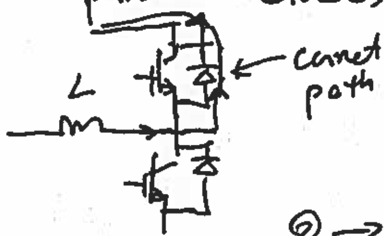
①: $T_1 T_2$ ON. Current path $T_1 T_2$ (back to start of the cycle)

(c) The current starts using paralled diodes during dead-time thus the ~~to~~ IGBTs are switching when zero voltge (current in the paralled diode, giving zero voltge across the transistor).



V_{CE} of IGBT is zero when switching on.

$E_{ON} = 0$. $P_{loss\,ON} = E_{on} \cdot f = 0$.

② → ③, ⑤ → ⑥ as (b)

d) $V_{AB} = \frac{4V_d}{\pi} \sum_{n=1,3,5\ldots}^{\infty} \frac{\sin(n\omega t)}{n}$

when $n=1$, $V_{AB1} = \frac{4V_d}{\pi} \sin n\omega t$

$V_{AB1rms} = \frac{2\sqrt{2}V_d}{\pi}$

e) $M = 90\%$

$\hat{V}_{AB1} = 0.9 V_d$, $V_{AB1rms} = \frac{0.9}{\sqrt{2}} V_d = 0.636 V_d$

The harmonics of uniplolar PWM starts at 2 times of switching frequency $2\omega_s$. The harmonics of biplar PWM starts at the switching frequency ω_s. If the switching frequency is the same, less inductance L_f is required for unipolar PWM due to higher cutting frequency of the filter.