Version RAM/3

EGT2
ENGINEERING TRIPOS PART IIA

Wednesday 30 April 2014 9.30 to 11

Module 3B3

SWITCH-MODE ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) An LED lamp for use at 230 V 50 Hz has the circuit of Fig. 1, with an equivalent resistance of 2.3 kΩ and the smoothing capacitor is 4.7 μF, rated at 400 V.

(i) State a simplified expression for the ripple voltage on the capacitor based on instantaneous charging of the capacitor. [5%]

(ii) Estimate the voltage ripple, stating any additional assumptions made. [5%]

(iii) Making reference to a sketch of the capacitor voltage waveform, show that the expression stated in (i) above is not appropriate in this case. [15%]

(iv) Estimate the duration of the rectifying diode *on-time* and the ripple in the LED current. [35%]

(v) Suggest two reasons why the circuit in Fig. 1 has been chosen. [10%]

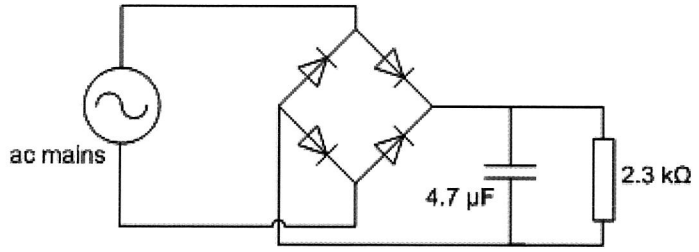

Fig. 1

(b) A triac dimmable lamp employs an integrated circuit. The input circuit of the lamp uses a bridge rectifier but without a smoothing capacitor.

(i) Why is the smoothing capacitor omitted? [5%]

(ii) If the circuit acts to control the lamp's current, hence brightness, in proportion to the mean voltage at the output of the bridge rectifier, find the range of triac firing delay angles to reduce the brightness to 10% of full output. [15%]

(iii) For start up, a linear regulator is used to give the controller a DC supply of 14 V nominal. Once operating, the DC supply is derived from the switch-mode circuit (a fly back converter) controlling the lamp current. Also the voltage across the LEDs is nearly constant over the normal range of operating currents. Why is this an advantageous arrangement? [10%]

2 (a) Give two reasons why a flyback converter is a good choice of circuit for a computer power supply. [10%]

(b) With the aid of diagrams show the relationship of primary transformer voltage, the current in the magnetizing inductance and the secondary diode current. The transformer may be represented by an ideal transformer with a magnetizing inductance referred to the primary of L_o as shown in Fig. 2. Continuous conduction can be assumed.

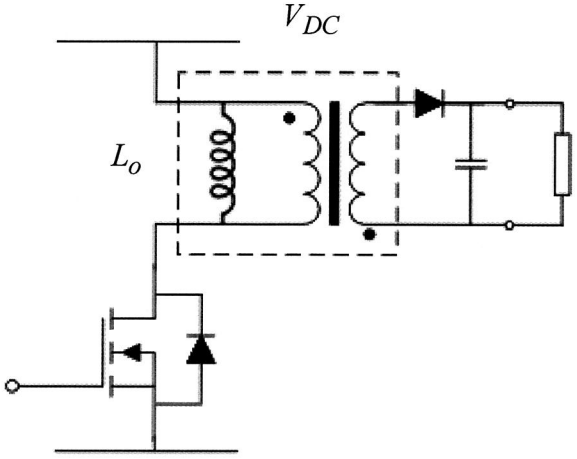

Fig. 2 [25%]

(c) Show that the output voltage, assuming an ideal diode, is given by

$$V_o = V_{DC} \frac{N_2}{N_1} \left(\frac{\rho}{1-\rho} \right)$$

where ρ is the duty cycle and N_1 and N_2 are the primary and secondary turns respectively. [20%]

(d) (i) If the power supply is to work in all countries, with the DC input varying from 140 V to 360 V, suggest a suitable turns ratio and range of duty cycles to achieve a 5 V output under all circumstances. The practical range of allowable duty cycles is 0.2 to 0.8. [25%]

(ii) Explain why very small or very high duty cycles are undesirable. [10%]

(iii) What is the minimum voltage rating of the transistor for your design? [10%]

3 (a) Three-phase bridge inverters with pulse width modulation are widely used for motor drives. For the following applications suggest an appropriate switching frequency and modulation scheme, giving brief reasons for your choices.

(i) An inverter for a domestic heat pump with a motor rated at 6 kW. [10%]

(ii) A general purpose industrial drive rated at 50 kW. [10%]

(iii) A railway traction drive rated at 1 MW. [10%]

(b) (i) Table 1 shows the allowable states of the switches for the three-phase full bridge inverter shown in Fig. 3. Making reference to this table explain how the circuit can function as an inverter and how the magnitudes of V_{AB},V_{BC} and V_{CA} may be controlled.

State	'ON' switches	$\frac{V_A}{V_{DC}}$	$\frac{V_B}{V_{DC}}$	$\frac{V_C}{V_{DC}}$
V_1	S_1, S_6, S_2	1	0	0
V_2	S_1, S_3, S_2	1	1	0
V_3	S_4, S_3, S_2	0	1	0
V_4	S_4, S_3, S_5	0	1	1
V_5	S_4, S_6, S_5	0	0	1
V_6	S_1, S_6, S_5	1	0	1
V_7	S_1, S_3, S_5	1	1	1
V_8	S_4, S_6, S_2	0	0	0

Table 1

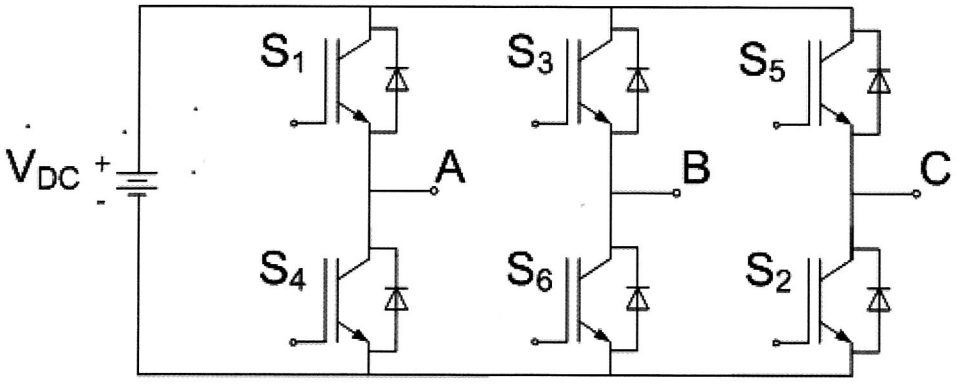

Fig. 3 [35%]

(ii) On a vector diagram indicate the zero states as well as the six switch states used for Space Vector Modulation (SVM). [10%]

(iii) What is meant by 'direct-direct' and 'direct-inverse' switching sequences? [10%]

(iv) For operation in the sector bounded by V_1 and V_2 show that the duty cycle for V_2 is given by

$$m \sin\theta$$

Where m is the modulation index and $m = 1$ is the largest circle that can be drawn inside a hexagon. [15%]

4 (a) List the key differences between unipolar and bipolar switching devices with regard to

(i) *on-state* performance [10%]

(ii) *switching losses* [10%]

using the MOSFET and IGBT as examples.

(b) Choose an appropriate transistor for use in the following applications and state briefly the reasons for your choice.

(i) The ballast circuit for a 20 W compact fluorescent lamp working from the single phase mains. [10%]

(ii) An inverter for motor drives up to 20 kVA working from a 400 V three-phase supply. [10%]

(iii) A 48 to 12 V DC-DC converter rated at 200 W with a switching speed of 100 kHz. [10%]

(c) (i) What is meant by a clamped inductive load? [10%]

(ii) On a diagram show the *gate-source* voltage, *drain-current* and *drain-source* voltage waveforms with their correct time relationship for the *turn-on* of an IGBT with a clamped inductive load. [20%]

(iii) An IGBT operates with a clamped inductive load with a constant load current of 20 A from a 300 V DC supply. The gate is driven via a resistor from a drive circuit with outputs of 0 and 12 V with negligible rise and fall times. Above the threshold voltage of the IGBT the current is given by

$$I_c = 2.5(V_{GE} - 6)^2$$

Find a suitable value of gate resistance if a drain voltage fall time of approximately 50 ns is required. [10%]

The input capacitance C_{iss} is 1.6 nF and the reverse transfer capacitance C_{rss} is 50 pF.

(iv) What is the delay time between the rise in gate driver voltage and the start of the fall in drain voltage? [10%]

END OF PAPER

3B3 Numerical answers

1 (a) (ii)	298V
(iv)	4.1mx
(b) (ii)	0° to 143°
2 (d) (i)	turns ratios between 112:1 and 18:1 are possible with a turns ratio of 50:1, range of duty cycle is 0.41 to 0.64
(iii)	610 V for 50:1 turns ratio
4 (c) (iii)	10.6 Ω
(iv)	21.3 ns