Version AHG/2

EGT2
ENGINEERING TRIPOS PART IIA

Thursday 1 May 2014 9.30 to 11

Module 3F5

COMPUTER AND NETWORK SYSTEMS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) What is meant by a *load-store instruction set architecture*? How does the adoption of a load-store architecture influence the design of CPU hardware? [20%]

(b) Figure 1 shows the datapath and control for a single-cycle implementation of the MIPS instructions `lw sw add sub and or slt` and `beq`. The operation times of the main functional units are: 2 ns for the memory (read or write); 2 ns for the ALU and adders; and 1 ns for the register file (read or write). All other units have negligible latencies and there is no pipelining. How many instructions can be processed per second? [10%]

(c) Someone proposes an extension to the MIPS instruction set to include a new `add3` instruction, which sums three values simultaneously. For example:

```
add3 $19,$18,$17,$16     # $19 loaded with $18 + $17 + $16
```

(i) Explain how the `add3` instruction could be formatted in 32 bits, without breaking the regularity of the MIPS instruction set. [10%]

(ii) List carefully all the changes you would need to make to the datapath and control in Fig. 1 to accommodate the new `add3` instruction. You may introduce only multiplexors, connections, control signals and one more adder. You may also assume that the register file can be modified to output the contents of three registers simultaneously. [25%]

(iii) How many instructions can your modified datapath process per second? [10%]

(iv) With reference to Amdahl's Law, discuss how your modification is likely to impact on performance. [25%]

(cont.

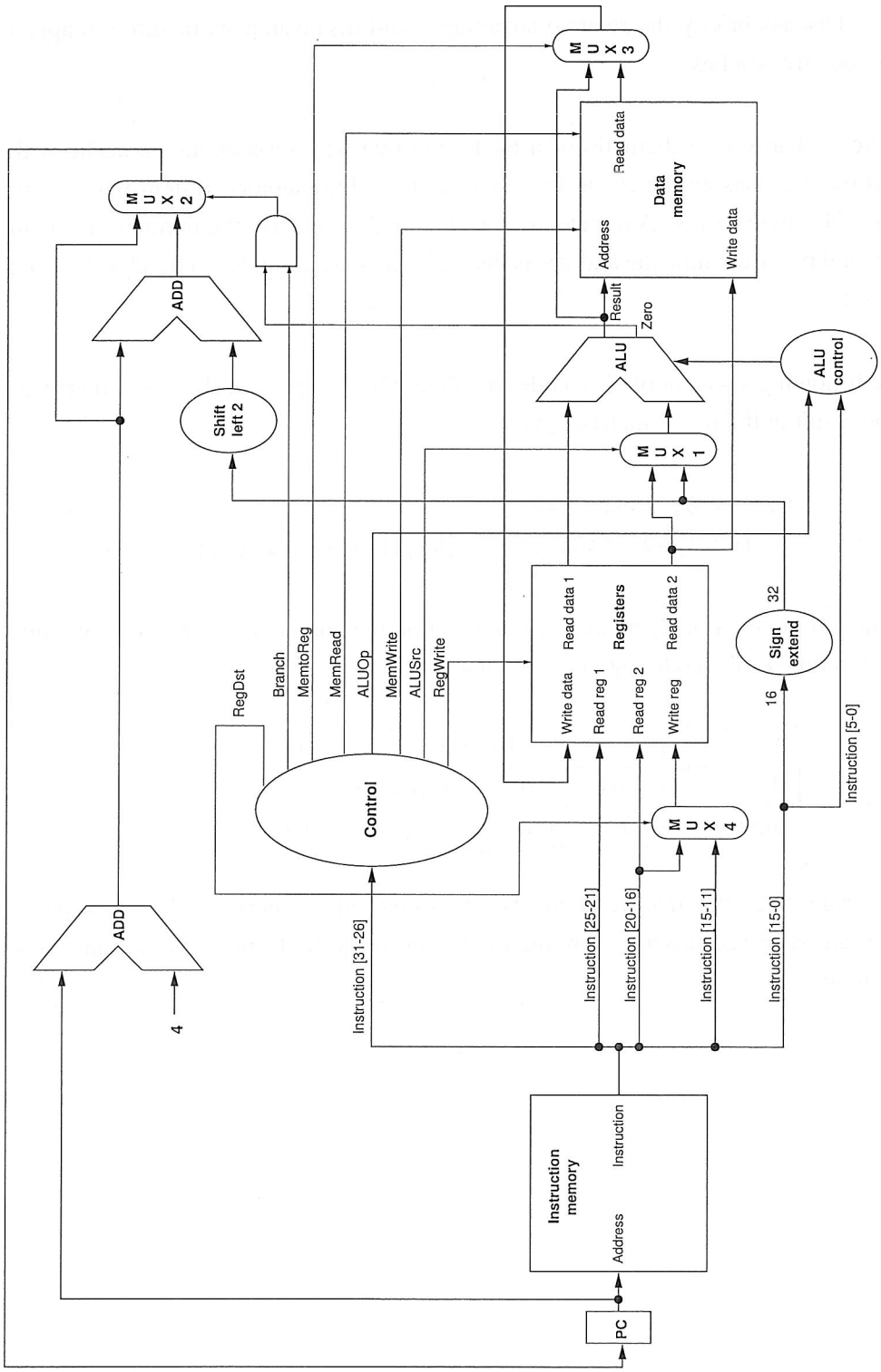
M U X 3
Read data
Data memory
Address
Write data
M U X 2
ADD
Result
Zero
ALU
ALU control
Shift left 2
M U X 1
Read data 1
Registers
Read data 2
Write data
Read reg 1
Read reg 2
Write reg
32
Sign extend
16
RegDst
Branch
MemtoReg
MemRead
ALUOp
MemWrite
ALUSrc
RegWrite
Control
M U X 4
Instruction [5-0]
ADD
4
Instruction [31-26]
Instruction [25-21]
Instruction [20-16]
Instruction [15-11]
Instruction [15-0]
Instruction memory
Instruction
Address
PC

Fig. 1

2 (a) Discuss briefly the relative advantages and disadvantages of direct mapped and set-associative caches. [20%]

(b) Sketch a hardware schematic of a 64 KByte two-way set-associative cache with four-word blocks. Design the cache for a byte addressable memory system with 32-bit addresses and 4-byte words. Annotate your sketch to show clearly the number of sets in the cache, and precisely how the address is divided into a tag, an index, a block offset and a byte offset. [40%]

(c) The following segment of C++ code calculates the transpose of the `R` $\times$ `C` matrix `a`, storing the result in the `C` $\times$ `R` matrix `a_t`.

```
for (i=0; i<R; i++)
   for (j=0; j<C; j++) a_t[j][i] = a[i][j];
```

Each element of `a` and `a_t` is one byte. Depending on the numbers of rows and columns, the execution time of the code segment is found to be:

R	100	2×10^7	2	100×10^7
C	2×10^7	100	100×10^7	2
time (s)	20.0	5.8	4.4	5.7

By considering how the matrix elements are stored in memory, and the order in which they are accessed, discuss how the execution times might be explained in terms of cache misses. [40%]

3 (a) There are two main types of service requirement that have greatly influenced the evolution of modern telecommunications and computer networks. Give a brief description of each requirement and describe the type of network connectivity and switching that is best suited to each one. Give an example of a modern network service which falls into both of the above categories and outline how well each requirement is met. [25%]

(b) One of the biggest evolutions in telecommunication networks was the plesiochronous digital hierarchy (PDH). Explain why the service requirement of telephony was a key factor in the creation of PDH and explain the significance of the 125 μs time period. [25%]

(c) PDH was eventually phased out in favour of the synchronous digital hierarchy (SDH). How did the service requirements of telephony make this a necessity? Draw a sketch of the STM-1 frame and explain why the shape of the frame is a vital part of the operation of SDH. Use the information in your sketch to calculate the fundamental data rate of a STM-1 transmission link. [30%]

(d) The majority of modern internet traffic is sent using the internet protocol (IP) over a transport technology such as Ethernet or Frame Relay. Do you think this sort of traffic can be reliably sent over SDH? Explain your reasoning. [20%]

4 (a) Define the purpose of the open systems interconnect (OSI) reference model. Sketch the model for two computers interconnected via a network. Explain how each layer passes information across the model. [30%]

(b) Describe the functions of layer 2 and layer 3 in the OSI model. Explain why layer 2 is split into two sub-layers when considering local area networks (LANs). [20%]

(c) One of the key features of the medium access control (MAC) sub-layer is the hardware address structure used in LANs and network equipment. What is the format of this address and why did it evolve in layer 2 and not layer 3? Is this layer really an appropriate place for this address? [30%]

(d) When using the transmission control protocol/ internet protocol (TCP/IP) in a LAN, one of the most important functions of a router is to convert between network and hardware addresses. How does this sort of process fit into the OSI and IP reference models? Identify a suitable protocol in the IP stack and briefly explain its function. What might happen if an unknown hardware address is received by the protocol? [20%]

END OF PAPER

Part IIA 2014

Module 3F5: Computer and Network Systems

Numerical Answers

1. (b) 125×10^6 instructions per second

   (c) (iii) 125×10^6 instructions per second

3. (c) 155 MBit/s