1. (a)

The properties of some of the WBG and UWBG materials are given below vs Silicon.

Physical Property	Si	4H-SiC	GaN	SC CVD Diamond	β-Ga_2O_3
Band gap (eV)	1.1	3.2	3.4	5.5	4.9
Relative permittivity	11.9	10	9.5	5.7	10
Breakdown field (MV/cm)	0.3	3	3.3	5	8
Thermal conductivity (W/K/cm)	1.48	3.30	1.30	24.00	0.13
Electron Mobility (cm^2/(Vs)	1350	700	2000(HEMT)	4500	200

(i) Dielectric mobility

Dielectric constant appears in the Ron vs BV (breakdown voltage) in the equation below. The higher the dielectric constant the lower Ron (beneficial). The dielectric constant also affects the capacitances. The lower the dielectric constant the lower the semiconductor. Silicon has higher dielectric constant than the other WBG but the effect is relatively small (except for Diamond). capacitances, resulting in higher speed.

$$R_{ON} = \frac{4\,BV^2}{\mu\,\varepsilon\,E_{max}^3}$$

(ii) Field strength (Critical Electric field)

The critical electric field (also known as field strength) is at least 10x higher for WBG and UWBG materials when compared to silicon. It is this fundamental property that makes a very compelling case to change from silicon to WBG and UWBG materials in power electronics. In the equation above a 10x increase in the critical electric field results in 10^3 decrease in the on-state resistance.

(iii) Electron and hole mobility

In the equation above the on-state resistance is inverse proportional to the mobility. The higher the mobility the lower the on-state resistance. The high 2DEG mobility in GaN devices is a particular advantage. Bulk SiC has lower mobility than both silicon and GaN. The hole mobility is only relevant for p-type power devices. The vast majority of power devices today are n-type.

(iv) Thermal conductivity

Higher thermal conductivity is beneficial to extract heat out of the device leading to lower operating temperature, which is good for reliability and more efficient operation. Diamond and SiC have very high thermal conductivity. GaO is very poor. [20%]

(b) $f = \frac{1}{T} = 20\text{kHz} \quad \Rightarrow \text{T} = 50\,\mu s, \qquad D = 50\%,$

$$DT = t_{on} + t_r + t_d = 25\mu s \Rightarrow t_{on} = 25 - 0.5 - 0.5 = 24\mu s$$
$$(1-D)T = t_{off} + t_s + t_f = 50\mu s \Rightarrow t_{off} = 25 - 1 - 1 = 23\mu s$$

ON -STATE

$P_{\text{ON}} = \frac{1}{T}\int_0^{t_{\text{ON}}} V_{\text{CE}} I_C dt = V_{\text{CE}} I_C \frac{t_{on}}{T} = 1 \times 100 \times 0.48 = 48W$

TURN – ON

$$P_d = \frac{1}{T}\int_0^{t_d} V_{dc}\, I_{OFF} dt = t_d f I_{OFF} V_{dc} = 4\, mW - \text{(can be neglected)}$$

$P_r = \frac{1}{T}\int_0^{t_r} I_C \frac{t}{t_r}[V_{dc} + (V_{CE} - V_{dc})\frac{t}{t_r}]\, dt = t_r f I_C \left[\frac{V_{dc}}{2} + \frac{V_{CE}-V_{dc}}{3}\right] = 67W$

TURN – OFF

Delay time: $P_s = V_{\text{CE}} I_C t_s f = 2W$

Current fall time:

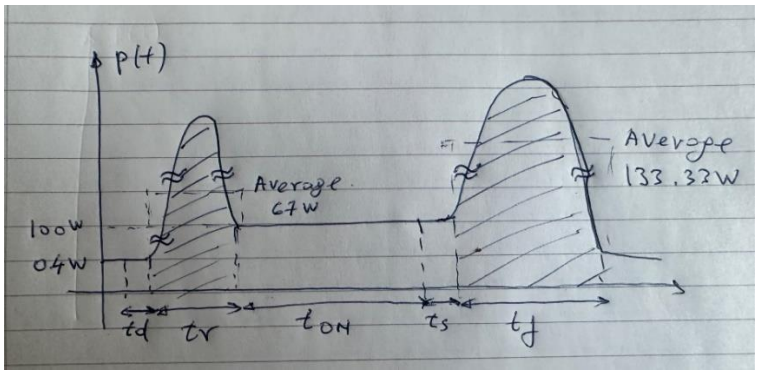
$P_f = \frac{1}{T}\int_0^{t_f} I_C(1 - \frac{t}{t_f}) V_{dc} \frac{t}{t_f} dt = t_f f I_C \frac{V_{dc}}{6} = 133.333W$

OFF -STATE

$$P_{OFF} = V_{\text{dc}} I_{\text{OFF}} t_{OFF} f = 0.184W$$

Total losses (on-state + turn-on + turn-off + off-state): P total= 48+67+ 2+ 133.33+ 0.184= 250.52W [30%]

(ii)



[20%]

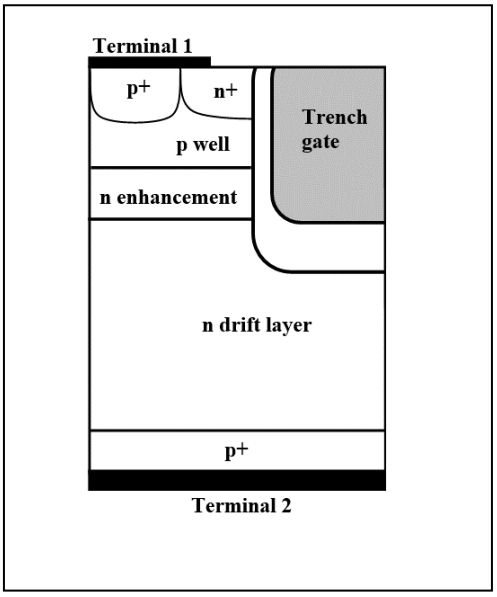
(iii)The power loss due to the base current can be calculated as:

$P_B = V_{BE} I_B D = 1.25W$ [10%]

(iv) The BJT can be operated in saturation with the base-emitter and base-collector junctions forward-biased and their voltage drops in the opposite direction and therefore cancelling each other. For this reason the VCE could be smaller than VBE. [10%]

(v) If a silicon transistor is used, the drift region (the collector region) would be significantly longer. The on-state losses would be much higher and the speed would be lower resulting in higher switching losses too. [10%]

2.



Terminal 1 – Cathode/Emitter, Terminal 2 – Anode/Collector. This is a NPT Trench IGBT type structure with bipolar conduction and controlled through the potential applied to the insulated trench gate.

The device is made in Silicon Carbide which means the drift region (base of the PNP transistor) is thin and the gain is expected to be higher. This is advantageous in the on-state, but the field in the drift region is very high putting pressure on the trench oxide. Additionally, this device can only be useful for the very high voltage ranges (above 10kV). This is because the p+/n drift junction (anode junction) cannot open below ~2.5 V (typical opening of a junction in SiC) and this limits the minimum achievable voltage drop in the on-state (thus limiting the on-state efficiency of

- The turn-on : Vgs >Vth such that a channel is formed on the side walls of the trench and allowing electrons top flow from the cathode terminal through the channel formed in the p-well into the n-enhancement layer n-layer (drift region). Thus electrons are injected in to the base (n drift region) of the P+/n-drift/p well transistor, modulating the conductivity of the drift region.
- In the on-state, the voltage drop is the sum of the anode junction voltage drop ~ 2.5 V, the voltage drop across the modulated n drift layer and the voltage drop across the channel.
- In the off-state, the device is blocking the voltage due to the action of the depletion region extending into the n-layer (generated across the reverse biased p-well/n layer junction). In this mode Vgs <Vth
- In the turn-off, the channel is stopped by applying Vgs <Vth. The turn-off speed is limited by the clearance of the plasma in the drift region and by the internal parasitic capacitances

The thick oxide at the bottom of the trench has a dual purpose (i) it protects the trench corner and the trench bottom as the field in the oxide is smaller which results in in better reliability (less probability of dielectric breakdown, no tunnelling through oxide and no hot carrier injection) (ii) reduces the Miller (gate-drain) capacitance by increasing the thickness of the dielectric present between the Gate and the drift region.. [30%]

(b) The enhancement layer acts as an electron emitter injecting electrons from the top of the device into the drift region. This ensures high level of plasma (high conductivity modulation) at the top of the drift region, resulting in lower on-state voltage, and consequently lower on-state losses. There is however a trade-off regarding the doping level of the n enhancement layer. On one hand the n

enhancement layer needs to be highly doped to increase the electron injection and thus reduce the voltage drop in the on-state but on the other hand it needs to be relatively lowly doped to be completely depleted and allow the depletion region to extend farther into the n drift layer during off-state (voltage blocking mode). The n enhancement also helps spreading electron current more efficiently. [20%]

(c)

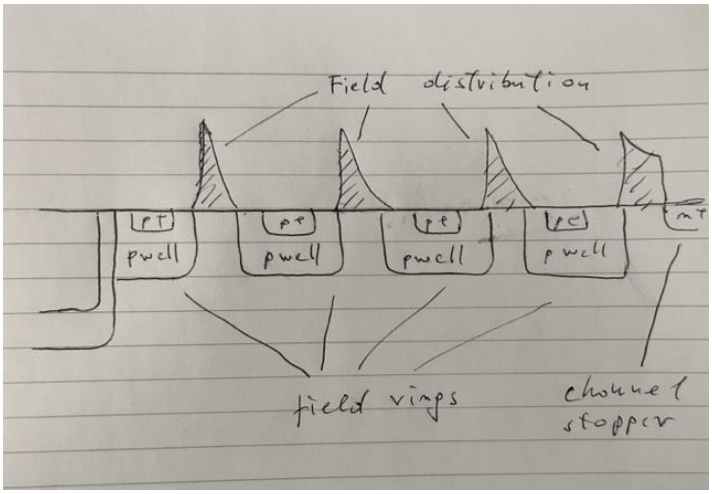
Advantages:

- The thick oxide reduces the Miller capacitance (allowing for faster dV/dt transients) and results in lower oxide fields (enhanced reliability)
- This an IGBT and therefore higher current densities are expected. The device should be more efficient for very high voltage ratings, in excess of 10 KV,

Disadvantages:

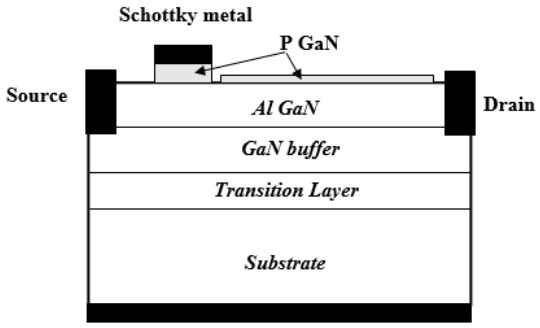
- Depositing or growing a different oxide thickness on the bottom of the trench to that of the side walls is challenging. .
- The IGBT is slow and therefore the switching speed is limited. Losses are high especially during turn-off [25%]
- In the off-state there is a minimum voltage drop of 2.5 V associated with the anode junction. Therefore the device is not suitable below voltage ratings of 10 kV, as the on-state losses are too high.

(d)



The ring termination could use a combination of floating rings made of p well and p+ layers (same as in the active area). The field is distributed between the rings and for an optimal distribution the peak levels should be approximately equal. The cumulative area under the multiple field shapes, when at least one the peaks reaches the avalanche level, is the breakdown voltage. Other termination designs are possible, using for example p well and field plates, or using floating field trenches. [25%]

3. (a) The device is based on a Two Dimensional Electron gas (2DEG) formed between a GaN buffer and an AlGaN layer placed on top. The electrons flow from the source to the drain (current flows in the opposite direction) through the 2DEG layer. The gate modulates the flow of the electron current through the 2DEG and is used to turn on or turn off the device. The gate is based on a p-GaN gate to achieve a normally off behaviour (enhancement mode). The device is turned off or in the off-state when the gate potential applied to the gate with respect to the source is smaller (more negative) than the threshold voltage. Typical threshold voltages for the p-GaN gate structure are in the range of 1 to 1.7V. In the off-state the device can block high voltages applied to the drain, thanks to the high field strength (critical electric field) in GaN. The extra p-GaN creats a RESURF type (or superjunction type effect). Partial charge balance is achieved between the negative fix ion charge in the extra pGaN layer (which is depleted during off-state) and the positive piezo--polarization charge present at the GaN/AlGaN heterojunction, when the 2DEG is depleted in the off-state.



[35%]

(b) In p-GaN Gate technology the maximum positive gate-source voltage is limited by the steep increase in the gate current. There are two back to back diodes (pGaN Gate/Schottky and p-GaN/2DEG). The p-GaN/Schootky diode is reverse biased when a positive potential is applied to the gate with respect to the source. Tunnelling through this diode becomes very strong at over 7V resulting in high gate leakage current. The negative gate value of VGS is limited by the leakage or avalanche of the pGaN /2DEG diode. Below the threshold voltage the 2DEG is depleted and the depletion region extends into the AlGaN and GaN layers. The maximum negative voltage depends on the pGaN doping, and the thicknesses of the AlGaN and GaN layers. Typical values are -30 to -50V. [15%]

(c) Advantage1 : GaN is wide bandgap material which offers much higher critical electric field than silicon. Hence the dimensions of a HEMT are much smaller for the same rated voltage. This results in much lower on-state resistance and potentially lower cost and cheaper packaging.
Advantage 2: The GaN device has high electron density (1e13 cm-2) and high channel mobility in the 2DEG (~ 1700 cm2/Vs)
Advantage3 : As the GaN is a significantly smaller device, the capacitances (input, Miller and output) are much smaller than in the large silicon RESURF devices. This means that the switching speed of GaN devices could be very high.

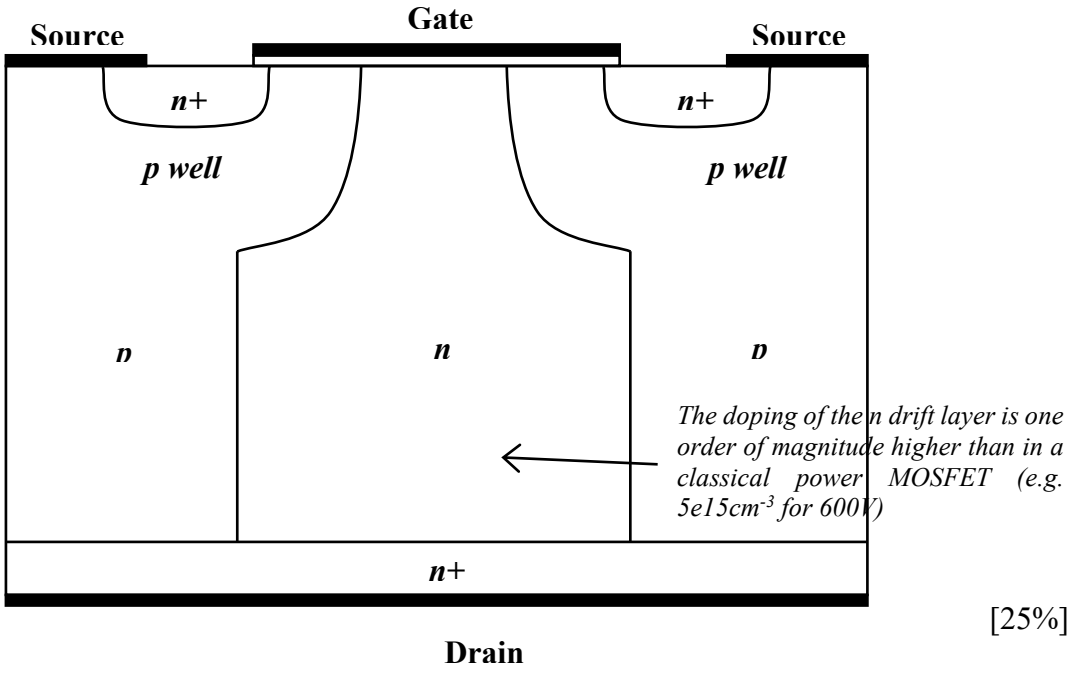
Disadvantage 1: Initial cost of the wafers. The technology is still expensive as it requires GaN epi layers to be grown on silicon substrates. [15%]

(d) The 2DEG is formed of electrons attracted to the GaN/AlGaN heterojunction interface to balance the existing positive piezo-polarization charge. The polarization charge is given by the difference in the polarization charge of the AlGaN and GaN. In addition to the polarization charge, there is a piezoelectric charge due to the mechanical stress created by longitudinal compression of AlaGaN layer to adapt to the thicker GaN layer.
Advantages (i) The 2DEG electron charge is a quantum layer confined at the interface and its electron charge balances out the piezo-polarization charge and needs no fixed ions, which means no scattering of electrons with heavy atoms is present resulting in high mobility.
(ii) no implantation process is needed to form this layer which naturally comes at the heterojunction interface and its strength can be accurately controlled by the Al mole fraction of the AlGaN layer and the thickness of the AlGaN (assuming GaN is a much thicker layer). [20%]

(e) Silicon – cheap, widely available and good foundry infrastructure, reasonably good thermal conductor.
Sapphire – insulating and enable high voltage breakdown. Good for multiple integration of dies. No transition layer needed as good lattice match to GaN. More expensive than silicon, and poorer thermal conductivity.
Semi-insulating Silicon Carbide – excellent thermal conductivity, and good isolation, allowing multiple die integration and enabling high breakdown voltage. Good lattice match to GaN. No need for transition layer. Most expensive of all substrates. [15%]

4. (a) (i) The Cool MOS is based on the superjunction effect. The superjunction comprises multiple junctions incorporated within the drift region with alternate layers of relatively highly doped n and p layers. The drift region is therefore made of thin and highly doped n/p pillars rather than a single n- layer. The depletion of the drift region is in this case dictated by these n/p multiple junctions rather than by the classical 1D p+/n- junction. Since the pillars are very thin (compared to their length), they deplete at much lower voltage (due to the extension of the depletion region across the n/p junctions). The net advantage is a major reduction in the on-state resistance for the same breakdown voltage. The electric field distribution is rectangular rather than triangular, and the doping levels of the n pillars is considerably higher than that of the classical power MOSFET. For the same breakdown a reduction of 5-10 times in the on-resistance is possible.

The Cool MOS is shown below:



[25%]

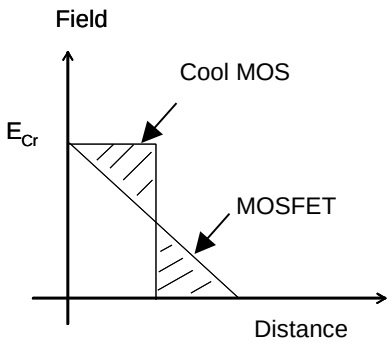
(b) (i)

For MOSFET $w = w_{drift}$ (the depletion region at breakdown just reaches the n+ drain region)

For the SiC MOSFET, the NPT designs gives $V_{BR} = \frac{E_{crSiC}}{2} w_{driftSiC}$.

$V_{BR} = \frac{\varepsilon_0 \varepsilon_{rSiC} E_{crSiC}^2}{2qN_{DSiC}} \Rightarrow N_{DSiC} = \frac{\varepsilon_0 \varepsilon_{rSiC} E_{CRSiC}^2}{2qV_{BR}}$ where E_{crSiC} is 10 times higher than E_{crSi} [20%]

(ii) The Cool MOS has an ideal rectangular distribution of the electric field compared to triangular field of a classical MOSFET:



$W_{driftSilicon\ CoolMOS} = \frac{W_{driftSilicon\ MOSFET}}{2}$ (the drift width of CoolMOS is only half of that of MOSFET. The drift region thickness of a classical MOSFET is $w = \frac{2V_{BR}}{E_{cr}}$

As the critical electric field is 10x higher in SiC than in Silicon, for the same breakdown voltage, it means that a classical power MSOFET in SiC would have a 10x decrease in thickness when compared to classical MOSFET. Hence the SiC Power MOSFET would have a 5X thinner drift region than a Silicon Cool MOS ($W_{driftSiliconCoolMOS} = 5W_{driftSiC}$) [25%]

(iii) specific resistance for Cool MOS $= \frac{W_{CoolMOS}}{q\mu_n N_{D_{CoolMOS}}} \frac{X_n}{X_n + X_p}$

$N_{D\ Cool\ MOS} = 10\times N_{D\ MOSFET}$

$X_n = 1/2X_p$ (to allow charge balance in the drift region of the Cool MOS)

$\frac{R_{spSiliconCoolMOS}}{R_{spSiliconMOSFET}} = \frac{1}{10} \times 3 \times \frac{1}{2} = \frac{3}{20} = 0.15$

From Rsp- V_{BR} equation, $\frac{R_{spSiliconMOSFET}}{R_{spSiCMOSFET}} = \frac{\varepsilon_0 \varepsilon_{rSiC} E_{crSiC}^3}{\varepsilon_0 \varepsilon_{rSi} E_{crSi}^3} = 750$

That means that $\frac{R_{spSiliconCoolMOS}}{R_{spSiCMOSFET}} = 0.15\ x750 = 112.5.$

The significance of this is that even if the silicon CoolMOS provides a substantial decrease in the specific on-state resistance compared to a classical silicon power MOSFET, the SiC classical MOSFET would have still provide a much lower resistance (~100x smaller than the Silicon Cool MO). This makes a compelling case for SiC in power devices. Note that the result above assumes same mobilities for SiC and Si. In reality the SiC mobility is lower which would result in lower decrease in on-state resistance (~ 50x) but still v. substantial. [30%]