4B21 – Analogue Integrated Circuits – SOLUTIONS

Question 1

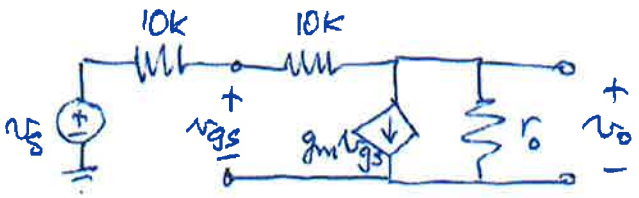
(a) Feeding back a portion of the output signal and combining it with the external input signal can be used to modify the characteristics of a circuit.

(b) The two kinds of feedback are Negative Feedback – used in amplifiers and control systems to improve performance – and Positive Feedback – used to create oscillators.

(c) (i)

Type of feedback arrangment: shunt-shunt (sampled signal = voltage, feedback signal = current)

(c) (ii)



(c) (iii)

$$\beta = -\frac{1}{10k} = -10^{-4}\ A/V$$

(c) (iv)

$I_D = K(V_{GS} - V_t)^2$ where $k = \frac{1}{2}\mu C_{ox}\frac{W}{L}$

Assume $0 \le V_t \le 2V$ and $0 < K \le 0.2\ mA/V^2$

(any values that fall in this range are acceptable)

We choose $V_t = 2V$ and $K = 0.125\ mA/V^2$

$1mA = 0.125 \times 10^{-3}\frac{mA}{V^2}(V_{GS} - V_t)^2 \Rightarrow (V_{GS} - V_t)^2 = 8$

So $(V_{GS} - V_t) = \pm\sqrt{8} = \pm 2.83V$

Hence $V_{GS} = 4.83V$ (since the other solution of $-0.83V$ does not turn on transistor)

Gain of transresistance amplifier is

$A = -g_m(10k \| 10k)(r_o \| 10k)$

Assuming $r_o >> 10k$, $A = -g_m(5k)(10k)$

$g_m = 2K(V_{GS} - V_t) = 2 \times 0.125 \times 2.83 = 0.71\frac{mA}{V}$

So $A = -0.71\frac{mA}{V} \times 5 \times 10^7\ V/A = -3.5 \times 10^4$

$$v_o/v_s = \left(\frac{A}{1+A\beta}\right)\left(\frac{1}{R_s}\right) = \frac{-3.5 \times 10^4}{1 + (-3.5 \times 10^4)(-10^{-4})} \frac{1}{10^4}$$

$$= -\frac{3.5}{4.5} = -0.79$$

$v_o/v_s = -0.79$ or -0.8

(c) (v)

Benefits:

- Increase in bandwidth
- Decrease in non-linear distortion
- Control over input and output impedances
- Desensitization of gain
- Decrease in noise

Drawback:

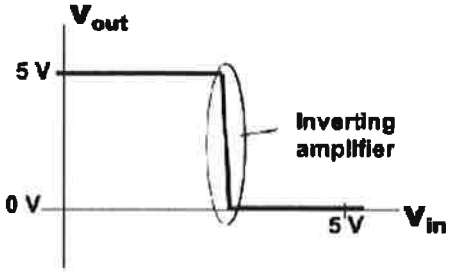
- Decrease in gain

Question 2

(a) Although the basic CMOS technology requires additional processing steps compared to the NMOS technology, it provides devices with complementary symmetry, i.e. p-channel transistors can be used as active loads in conjunction with n-channel transistors to obtain high voltage gain and DC level shifting.

(b)

The static operation of a generic CMOS inverter circuit is characterized by its voltage transfer characteristic. Here, if the input is HIGH (e.g., $v_{in} \sim 5$ V), the output is low ($v_{out} \sim 0$ V), and vice-versa. The logic inverter circuit is basically an inverting amplifier that is utilized in the extreme regions of operation whereby the transistors are in switch (on or off) mode. In the intermediate (or transition) region, however, such as at the output HIGH-to-LOW or LOW-to-HIGH transition, the inverter circuit behaves as an inverting linear amplifier with characteristic, $v_{out} = -Av_{in}$. Here, A is the circuit gain.



(c) (i)

For Q_2 to be saturated, we need $V_{DS} \leq V_{GS} - V_t$ where V_{GS} and V_t are negative. But $V_{DS} = V_{GS}$

$\Rightarrow V_{GS} \leq V_{GS} - (-2) = 0$ ($\leq +2$, so Q_2 saturated)

Since Q_2 is saturated, $I_D = K(V_{GS} - V_t)^2$

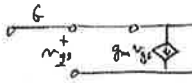
$V_{GS} = V_{DS} - \pm\sqrt{\frac{I_D}{k}} + V_t = \pm 5 - 2 = \begin{cases} 3\text{V} \\ -7\text{V} \end{cases}$

For Q_2 to be on, $V_{GS} < V_t$, so $V_{GS} = -7$V

So $V_{SG} = V_{SD} = 7$ V, hence $V_D = 10 - 7 = 3$ V

(c) (ii)

Equivalent circuit for Q_2 in this configuration is



labelling is same as NMOS because signals are ac

So the ac resistance between drain and source is $r_{ds} = \frac{v_{ds}}{i_{ds}} \simeq \frac{v_{gs}}{g_m v_{gs}}$ (if r_o omitted)

And $r_{ds} \simeq \frac{1}{g_m}$ for large r_o

(c) (iii)

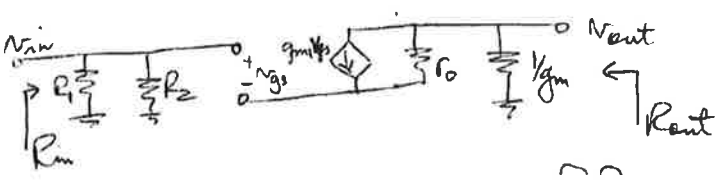
$r_o = |V_A|/I_D = 40\,k\Omega$

$g_{m1} = 2K(V_{GS} - V_t) = 0.2\times10^{-3}(7-2)$

$= 1$ mA/V

$g_{m2} = 2K(|V_{GS2}| - |V_t|) = 2\times0.1(7-2)$

$= 1$ mA/V



(c) (iv)

by inspection, $R_{in} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$

$= 4.8\,M\Omega$

R_{out} is obtained when $v_{in} = v_{gs} = 0$

$R_o = r_o // \frac{1}{g_m} \simeq \frac{1}{g_m}$

$= \frac{40\times1}{40+1}\,k\Omega = 0.98\,k\Omega$

$v_{out} \simeq -g_m v_{gs}\left(\frac{1}{g_m}\right) \simeq -v_{gs}$

$= -10^{-3} \times v_{in} \times 10^{3}$

$v_{out}/v_{in} = -1$.

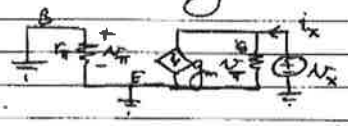
Question 3

(a) Ideal voltage source is one where the voltage across it is independent of the current through it. Ideal current source is one where the current through it is independent of the voltage across it.

(b) (i)

Output resistance when driven by ideal voltage source:

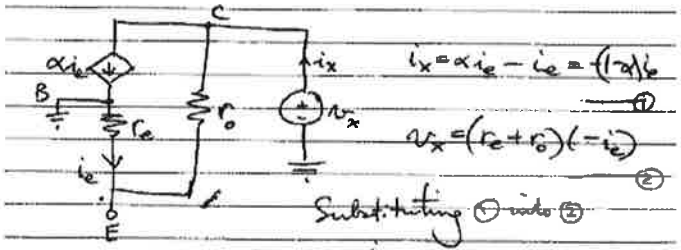
Use hybrid π: with test source at O/P and I/P s/c.



$v_x/i_x = r_{out}$; $i_\pi = 0$ and therefore

$r_{out} = r_o = 100\,k\Omega$

Output resistance when driven by an ideal current source - use T model with test source at O/P and current source becomes 0.



$i_x = \alpha i_e - i_e = -(1-\alpha) i_e$ — (1)

$v_x = (r_e + r_o)(-i_e)$ — (2)

Substituting (1) into (2)

$v_x = (r_e + r_o)\frac{i_x}{(1-\alpha)} \rightarrow v_x = (r_e + r_o)\frac{i_x}{(1-\alpha)}$

$v_x/i_x = r_{out} = \frac{r_e + r_o}{(1-\alpha)}$

But $(1-\alpha) = \frac{1}{\beta+1}$

Therefore $r_{out} = (\beta+1)(r_e + r_o)$

and $(\beta+1) r_e = r_\pi$

So $r_{out} = r_\pi + (\beta+1) r_o$

$= 1k + (101)(100k)$

$= 10.1\,M\Omega$

(b) (ii) The common-base amplifier, when driven by low source resistance, behaves as a voltage amplifier. On the other hand, with high source resistance, it behaves like a current follower. This transition takes place when the source resistance is at the vicinity of the emitter resistance, r_e.

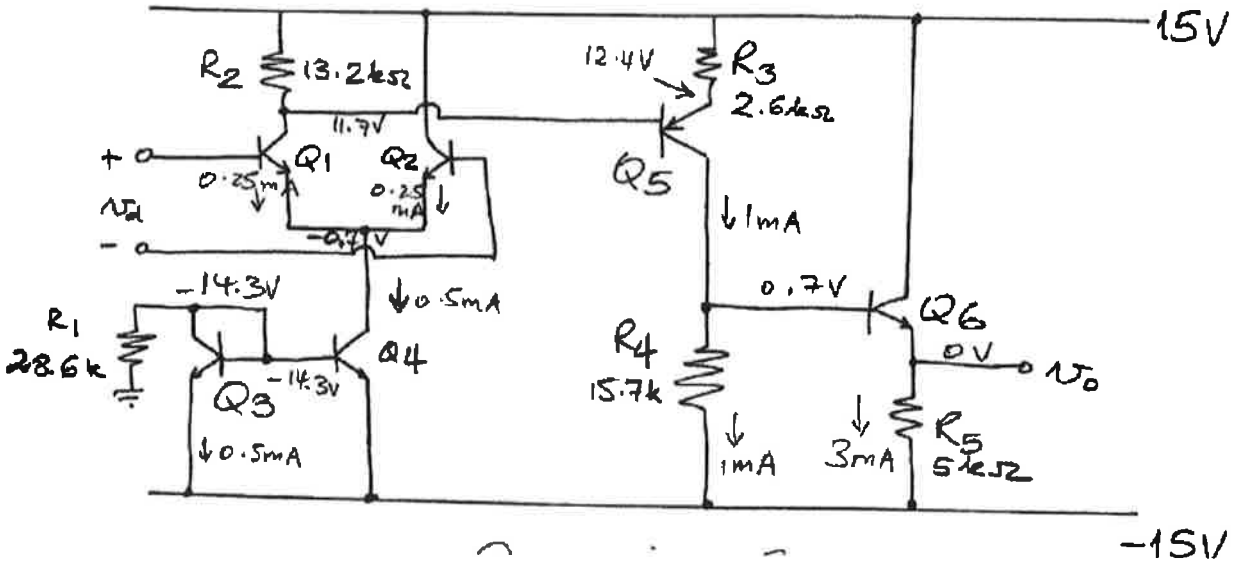
Question 4

(a) A multistage amplifier is formed by combining several several stages connected in a cascade – as in output of the first stage connected to form input of second stage and so on – to achieve the performance as required in many applications, which is otherwise not attainable with a single stage amplifier.

(b) If the gain of each amplifier stage is expressed in dB, then the total gain is the *sum* of the gains of the individual stages: Gain in dB (A) = $A_1 + A_2 + A_3 + A_4 + \ldots A_n$

(c) (i) Functionality of each transistor: Q3,4 – current source for biasing input stage, Q1,2 – input stage with differential in and single-ended out (i.e. differential to single-ended conversion), Q5 – DC level shifting, Q6 – emitter follower output stage.

(c) (ii) The DC voltages and currents are as indicated on circuit shown – assumptions used: $V_{BE} = 0.7V$ and negligible base currents.



(c) (iii)

Upper limit is set by Q1 and Q2

$V_B = V_C = 11.7V$

Lower limit is set by Q4 ; $V_{CQ4} = -14.3V$

So $V_{B1} = V_{B2} = -14.3V + 0.7V = -13.6V$

13.6V ≤ common mode range ≤ 11.7V

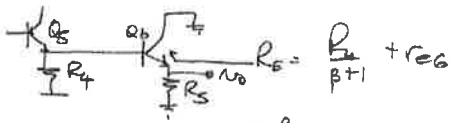
(c) (iv) Input and Output Resistance

$R_{in} = r_{\pi 1} + r_{\pi 2} = (\beta+1)(r_{e1} + r_{e2})$

$r_{e1} = r_{e2} = 25mV / 0.25mA = 100\Omega$

$R_{in} = 101 \times 200 = 20.2k\Omega$

Output Resistance, R_{out}



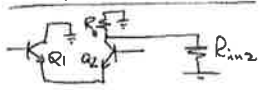
$R_5 = \frac{R_4}{\beta+1} + r_{e6}$

$R_{out} = R_S // \left[\frac{R_4}{101} + r_{e6}\right] = 5000 // 163.8$

$= 158.6\Omega$

Gain of the various stages

Gain of 1st (diff) stage



$R_{in2} = (\beta+1)(R_3 + r_{e5})$

$= (\beta+1)(R_3 + \frac{V_T}{1mA})$

$= 101\ (2.6k + 25.2)$

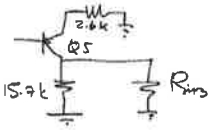
$= 265k\Omega$

Gain of diff. stage $= A_{V1} = \Sigma R_c / \Sigma R_E = \frac{R_2 // R_{in2}}{r_{e1} + r_{e2}}$

$r_{e1} = r_{e2} = \frac{25mV}{0.25mA} = 100\Omega$

$A_{V1} = -\frac{13.2 // 265k\Omega}{200\Omega} = -62.9\ V/V$

gain due to Q5



$R_{in3} = (\beta+1)(R_5 + r_{e6})$

$= 505.8 \times 10^3$

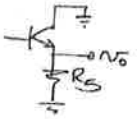
$r_{e6} = \frac{25mV}{3mA}$

$A_{V2} = -\frac{15.7k // 505.8k}{2.6k + r_{e5}}$

$r_{e5} = \frac{25mV}{1mA} = 25\Omega$.

$A_{V2} = -5.8\ V/V$

Gain of Q6



$A_{V3} = \frac{R_5}{r_e + R_5} = \frac{5000}{5000 + \frac{25}{3}}$

$= 0.998\ V/V$

Total Gain

$= A_{V1} A_{V2} A_{V3} = -62.9 \times -5.8 \times 0.998$

$= 364.1$ or $51\ dB$