Version AN/3

EGT3
ENGINEERING TRIPOS PART IIB

Tuesday 22 April 2014 2 to 3.30

Module 4B21

ANALOGUE INTEGRATED CIRCUITS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book
Attachments: Values of constants and relevant formulae (1 page)

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

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1 (a) What is feedback as applied to an electrical circuit? [10%]

(b) Name the two kinds of feedback arrangement used in electrical circuits along with one example of each. [10%]

(c) For the amplifier circuit and transistor parameter values given in Fig. 1, assuming mid-band frequency operation,

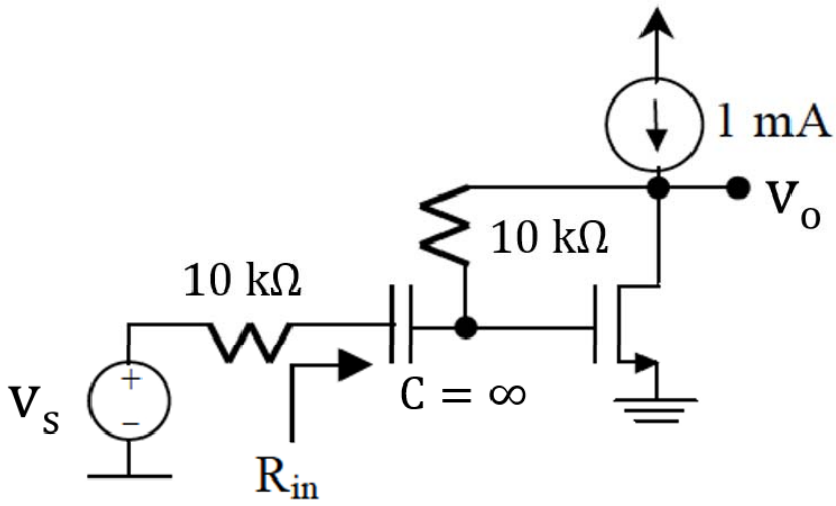

Figure 1

(i) Define the type of feedback arrangement. [10%]

(ii) Construct and label the small-signal equivalent circuit. [20%]

(iii) What is the value of the feedback network gain, β? [15%]

(iv) Using feedback techniques along with reasonable approximations, find the overall voltage v_o/v_s. State any assumptions made. [20%]

(d) List five benefits and one drawback of the above feedback arrangement. [15%]

2 (a) Why does the CMOS technology offer higher design flexibility for analogue functions compared to the NMOS technology? [20%]

(b) Describe the static operation of a generic CMOS inverter circuit aided by a sketch of its voltage transfer characteristic. [20%]

(c) For the CMOS amplifier shown in Figure 2 with the indicated values of components,

(i) Determine the DC value of the drain voltage V_D. [15%]

(ii) Show that the PMOS transistor Q_2 can be replaced by an ac equivalent resistance of approximately $1/g_m$. [15%]

(iii) Calculate the ac parameters and construct the small-signal equivalent circuit of the amplifier. [15%]

(iv) Calculate the amplifier's input resistance (R_{in}), output resistance (R_{out}) and the voltage gain (v_{out}/v_{in}) for mid-band frequency operation. [15%]

In your calculations, you can assume that $|V_t| = 2\ V, |V_A| = 100\ V,$ and $K = 0.1\ mA/V^2$ for both transistors.

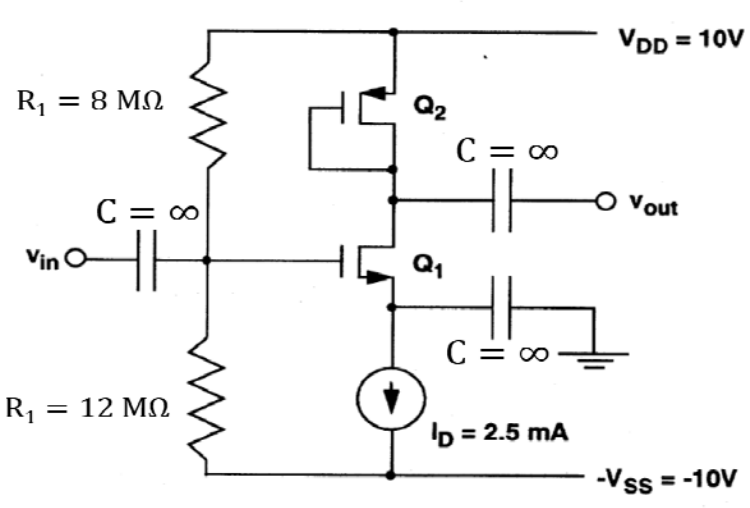

Figure 2

3 (a) Explain what is meant by an ideal voltage source and an ideal current source. [30%]

(b) Shown in Figure 3 are two common-base (CB) amplifiers, driven by (a) an ideal voltage source and (b) an ideal current source, respectively.

(i) Assuming that each circuit has been properly biased, and that the biasing networks, although not indicated in Fig. 3, do not affect the small-signal analysis, calculate the output resistance, $\boldsymbol{r_{out}}$ for circuits (a) and (b), using the following data: $r_\pi = 1\ k\Omega, r_o = 100\ k\Omega$, and $\beta = 100$. [50%]

(ii) Comment on the physical implications of the results for $\boldsymbol{r_{out}}$ for the two configurations. [20%]

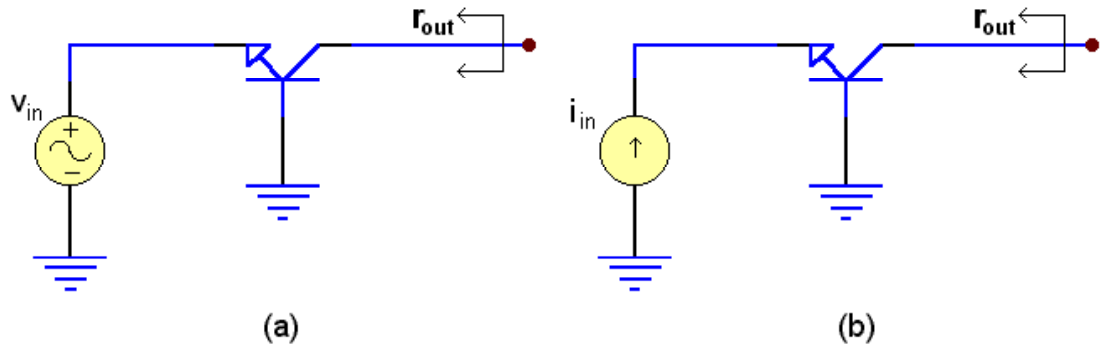

Figure 3

4 (a) Why are multi-stage amplifiers necessary from the standpoint of achieving the desired circuit characteristics? [15%]

(b) State the expression for the overall gain of a multistage amplifier of *n* stages, in decibels, expressed in terms of the gain of the individual stages. [10%]

(c) In the multi-stage amplifier circuit shown in Fig. 4,

(i) State the functionality of each transistor. [20%]

(ii) Calculate the necessary DC voltages and currents. Clearly state all assumptions. [20%]

(iii) What is the common-mode voltage range? [15%]

(iv) Find the input resistance, output resistance, and voltage gain (v_o/v_d). [20%]

Assume that all transistors are matched with $\beta = 100$ and $V_{BE} = 0.7$ V

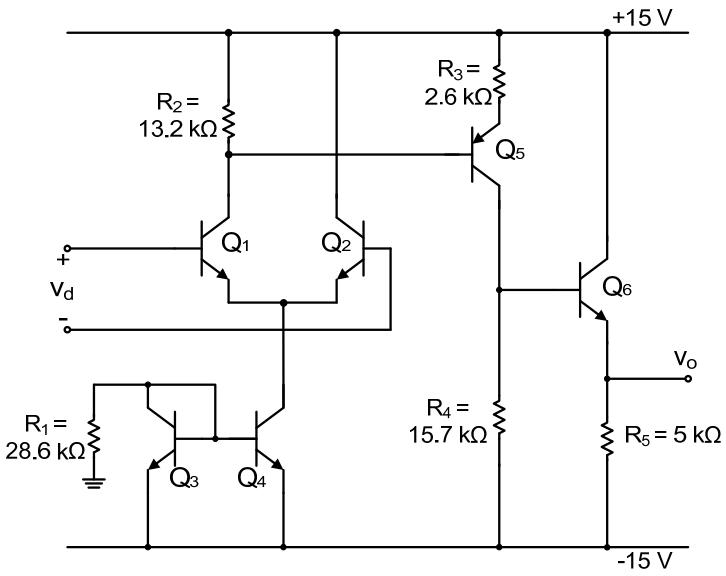

Figure 4

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FORMULA SHEET

Bipolar Junction Transistors:

$i_C = \alpha i_E \qquad i_C = \beta i_B \qquad i_B = (1-\alpha) i_E \qquad i_E = (\beta+1) i_B$

$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad V_T = \frac{kT}{q} = 25\ mV\ at\ 300K$

$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{V_T}{I_B} \qquad r_e = \frac{V_T}{I_E} \qquad r_o = \frac{V_A}{I_C}$

MOSFETs:

$i_D = K[2(v_{GS} - V_t)v_{DS} - v_{DS}{}^2]; \qquad i_D = K(v_{GS} - V_t)^2 = \frac{k'}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2$

$K = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right) \qquad k' = \mu C_{ox} \qquad g_m = 2K(v_{GS} - V_t) \qquad r_o = \frac{|V_A|}{I_D}$

Differential Amplifiers:

$v_o = A_d v_d + A_{cm} v_{cm}; \qquad CMRR = 20 \log|A_d / A_{cm}|$

$A_{cm} = \frac{v_o}{v_{cm}}$ ***or*** $A_{cm} = \frac{\Delta R_D}{2R}; \qquad A_d = \frac{v_o}{v_d} = g_m R_D$ ***or*** $A_d = \frac{\Sigma R_C}{\Sigma R_E}$

BJT small-signal operation: $i_{C1} \approx \frac{\alpha I}{2} + \frac{\alpha I}{2V_T}\frac{v_d}{2} \qquad i_{C2} \approx \frac{\alpha I}{2} - \frac{\alpha I}{2V_T}\frac{v_d}{2}$

$R_{id} = 2(\beta+1)(r_e + R_E) \qquad R_E = emitter\ resistance$

FET small-signal operation: $i_{D1} \approx \frac{I}{2} + \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2} \qquad i_{D2} \approx \frac{I}{2} - \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2}$

Millers Theorem: $C_{eq} = C_{bridge}(1-K) \qquad K \equiv \frac{V_2}{V_1}$