1. (a) The properties for Si and SiC are listed below.

Band gap (eV)	1.1	3.2
Relative permittivity	11.9	10
Breakdown field (MV/cm)	0.3	3
Thermal conductivity (W/K/cm)	1.48	3.30
Mobility (cm2/(Vs)	1350	700
Saturation velocity (107cm/s)	1	2

Silicon Carbide has a 10x increase in the critical electric field. The drift region can be made 100x more highly doped and 10x thinner in SiC than in Silicon. Taking into account that the mobility of SiC is ~1/2 of that of Silicon, the drift region resistance can be made ~ 500 x smaller in SiC than in Si. This results in lower on-state losses. This could also result in a smaller chip area which allows smaller capacitances and therefore faster speed. However the mobility in the SiC channel is 1/20 smaller than in Silicon. Below 100V, the channel resistance becomes a major part of the overall on-state resistance. Below 100 V, silicon trench MOSFETs are still very competitive. [20%]

(b) (i) $f = \frac{1}{T} = 100\,\text{kHz} \Rightarrow \text{T} = 10\ \mu s$, $D = 50\%$,

$$DT = t_{on} + t_r + t_d = 5\mu s \Rightarrow t_{on} = 5 - 0.5 - 0.1 = 4.4\mu s$$

$$(1-D)T = t_{off} + t_s + t_f = 5\mu s \Rightarrow t_{off} = 5 - 0.5 - 0.3 = 4.2\mu s$$

ON -STATE

$$P_{\text{ON}} = \frac{1}{T}\int_0^{t_{\text{ON}}} \text{V}_{\text{CE}} I_{\text{C}}\, dt = V_{\text{CE}} I_{\text{C}} \frac{t_{on}}{T} = 2 \times 100 \times 0.44 = 88W$$

TURN – ON

$$P_d = \frac{1}{T}\int_0^{t_d} V_{dc} I_{OFF}\, dt = t_d\, f I_{OFF} V_{dc} = \ 2.5\ \text{mW} \quad \text{(can be neglected)}$$

$$P_r = \frac{1}{T}\int_0^{t_r} I_C \frac{t}{t_r}[V_{dc} + (V_{CE} - V_{dc})\frac{t}{t_r}]dt = t_r\, f I_C[\frac{V_{dc}}{2} + \frac{V_{CE} - V_{dc}}{3}] = \ 9\text{W}$$

TURN – OFF

Delay time: $P_s = V_{\text{CE}} I_{\text{C}} t_s f = 10W$

Current fall time:

$$P_f = \frac{1}{T}\int_0^{t_f} I_C\left(\frac{t}{tf}\right)[V_{dc}\frac{t}{tf}dt = t_f\, f I_C \frac{V_{dc}}{6} = \ 27\text{W}$$

OFF –STATE

$P_{OFF}=t_{OFF}\ f\ V_{dc}I_{OFF}$= 21mW (negligible)

Total losses (on-state + turn-on + turn-off):

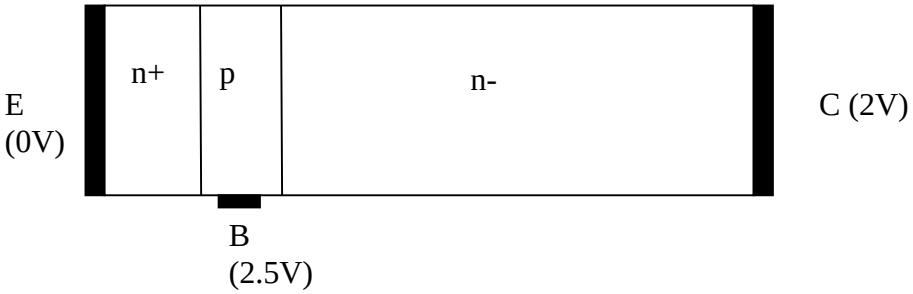
P total= 88+9+37= 134W

[40%]

(ii) The power loss due to the base current can be calculated as:

$$P_B = V_{BE} I_B D = 2.5W$$ [10%]

(iii) The structure is shown schematically below:



The device is made of a wide bandgap material – Silicon Carbide. This is why V_{BE} is 2.5 V (in Silicon is normally around 0.7V). The base collector junction is also forward-biased (just below 2.5V) and the 2V on-state voltage is mainly dropped across the collector region (as the base-emitter potential drop is almost cancelled out by the base-collector potential drop) . This region is relatively thick to withstand a large breakdown. In this case the breakdown voltage must be well in excess of the line voltage. The device operates in hard saturation during on-state to give a minimum voltage drop across the CE terminals.

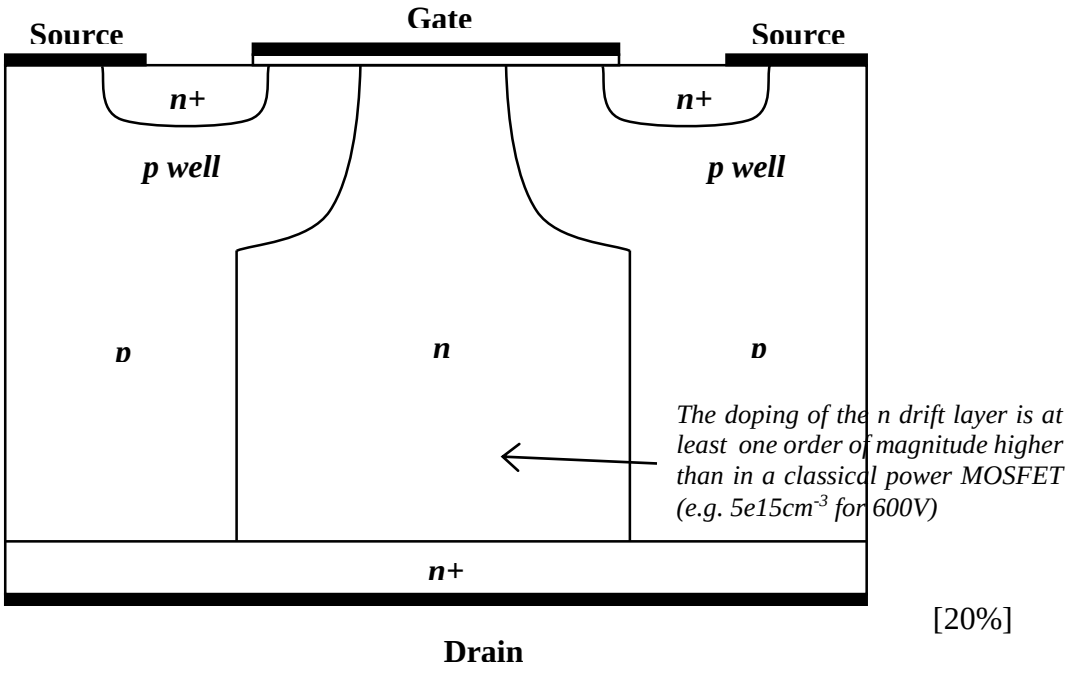
[20%]

(iv)The current gain is simply: I_C/I_B =50. This is significantly larger than in silicon devices which have a current of typically under 10 for high voltage devices (e.g. 600V). The reason is that the n- drift region (the collector region) is significantly thicker in silicon, decreasing the gain. The base in SiC can also be made thinner and more highly doped to avoid punch-through but without the risk of avalanche as the critical electric field in SiC is ~ 10 times higher than that in Silicon

[10%]

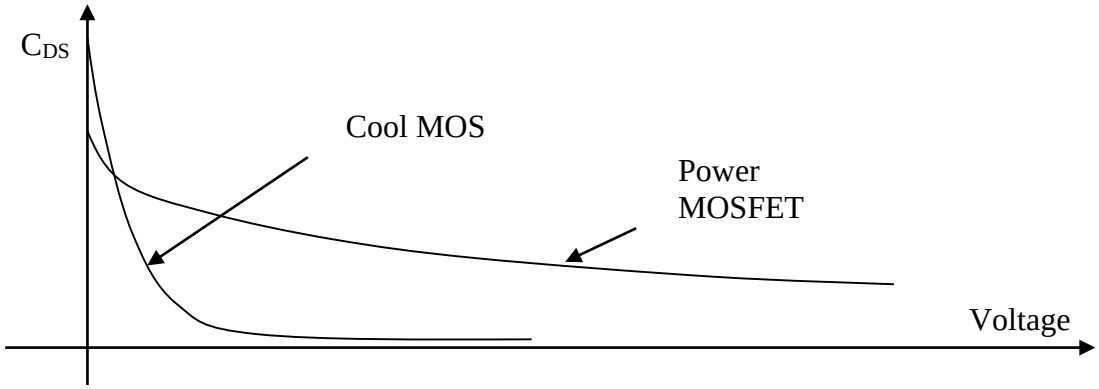
2. (a) (i) The Cool MOS is based on the superjunction effect. The superjunction comprises multiple junctions disposed in the drift region with alternate layers of relatively highly doped n and p layers. The drift region is therefore made of thin and highly doped n/p stripes rather than a single n- layer. The depletion of the drift region is in this case dictated by these n/p multiple junctions rather than by the classical p+/n- junction. Since the stripes are very thin (compared to their length), they deplete at much lower voltage (due to the extension of the depletion region across the n/p junctions). The net advantage is a major reduction in the on-state resistance for the same breakdown capability. The electric field distribution is square rather than triangular, and the doping of the n pillars is considerably higher than that of the classical power MOSFET. For the same breakdown a reduction of 5-10 times in the on-resistance is possible.

The Cool MOS is shown below:



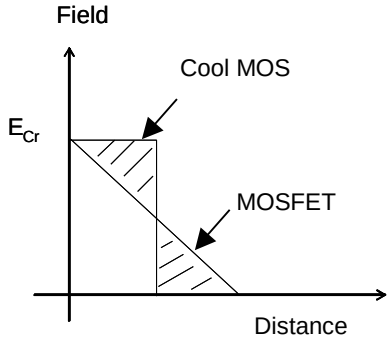
[20%]

(ii) The C_{DS} capacitance for the Cool MOS is high to start with, as the multiple junctions have a large (folded) area. At the same time the doping of the n and p pillars are very high limiting the extension of the depletion region at low voltages. These 2 effects lead to very high C_{DS} in Cool MOS at low voltages. At high voltages, in Cool MOS, the whole n-p pillar stack depletes, thus reducing sharply the capacitance. In contrast in Power MOSFET, the capacitance at low voltages is quite low (reduced area and reduced doping), while decreasing with $1/V^2$ at high voltages.



[25%]

(b) (i) For MOSFET $w = w_{drift}$ (the depletion region at breakdown just reaches the n+ drain region)



$$V_{BQ} = \frac{E_{cr}}{2} W$$

$$V_{BR} = \frac{\varepsilon_0 \varepsilon_r E_{cr}^2}{2qN_D} \Rightarrow N_D = \frac{2qV_{BR}}{\varepsilon_0 \varepsilon_r E_{CR}^2}$$

drift length $w = \frac{2V_{BR}}{E_{CR}} \Rightarrow w_{drift} = w = \frac{\varepsilon_0 \varepsilon_r E_{CR}}{qN_D}$ - MOSFET

$w_{drift\_CoolMOS} = \frac{w_{drift\_MOSFET}}{2}$ (the drift width of CoolMOS is only half of that of MOSFET , as the field distribution for Cool MOS is rectangular rather than triangular – see picture above) [25%]

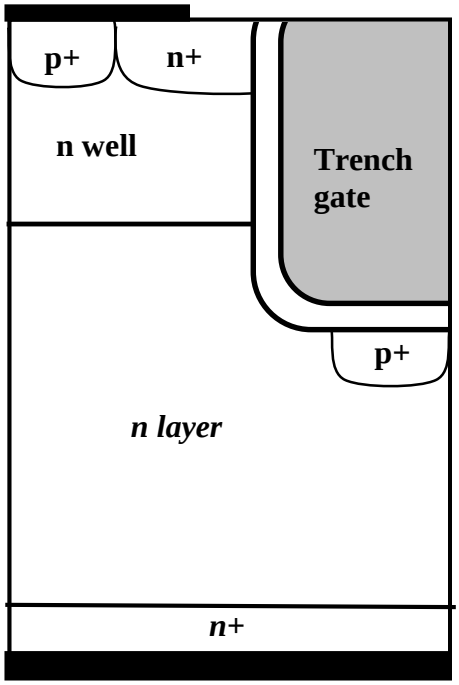
(ii) specific resistance for Cool MOS = $\frac{W_{CoolMOS}}{q\mu_n N_{D_{CoolMOS}}} \frac{X_n}{X_n + X_p}$

$N_{D\ Cool\ MOS} = 20 \times N_{D\ MOSFET}$ and $X_n = 1/4\ X_p$ (to allow charge balance in the drift region of the Cool MOS – total charge in n-pillar should equate the total charge in the p-pillar)

Rsp-Cool MOS/Rsp-MOSFET = (1/20) x 5 x (1/2) = 0.125 [20%]

(iii) Superjunction type structures such as Cool MOS have evolved by shrinking the dimensions of the pillars (stripes) and maintaining charge balance. The smaller the pillar width, the higher the doping. By maintaining a constant ratio and charge balance between the n-pillar and p-pillar widths and by increasing the doping of the n-pillar (while reducing its width), the on-state resistance (and hence the on-state losses) can be cut. In theory, the pillar width can go below 0.5 um. At very low width, the parasitic JFET effect (the depletion region associated with the p-pillar/npillar junction) starts to become important as it obstructs current flow through the n-pillar. [10%]

3. (a)



Terminal 1 – Source, Terminal 2 – Drain. This is a Trench MOSFET type structure and controlled through the potential applied to the insulated trench gate.

It can be a normally on device, but in this case it requires the p+ to beconnected to a terminal and a negative voltage applied to it to block the voltage

Or it can be a normally-off device, if the trenches (and adjacent p+ layers) are very close and the p+ layer under the trench is connected to ground (via a terminal), creating a strong JFET effect which allows the voltage to be blocked

- The turn-on is based on applying a step of Vgs >Vth such that a channel is formed on the side walls of the trench and allowing electrons top flow from the source terminal through the channel formed in the p-well into the n-layer (drift region) and to the n+ contact.
- In the on-state, the gate potential remains high and in the linear region the device behaves as a resistance. The dominant resistances are the channel resistance and the drift resistance. The parasitic JFET resistance can also be high (due to the p+ /n-layer being reverse biased when the p+ is connected to a terminal and grounded). To minimise this JFET resistance, the terminal connected to the p+ layer can be connected to a positive potential to mildly forward-bias the p+/n-layer junction to eliminate the depletion region or fully forward-bias the junction to inject holes and provide conductivity modulation. Controlling however, this terminal requires a drive circuit that is more complex.
- In the off-state, the device is blocking the voltage due to the action of the depletion region extending into the n-layer (generated at the reverse biased p+/n layer junction). In this mode Vgs <Vth (see comment above on normally-on versus normally-off device)
- The turn-off, the channel is stopped by applying a step of Vgs <Vth. The turn-off speed is limited by the internal parasitic capacitances [30%]

(b) The p+ role under the trench has a triple purpose (i) it provides the p-n junction to block the voltage. This assumes that the p+ layer is connected to a terminal and thus the p-n junction can be reverse biased. (i) it protects the trench corner and the trench gate dielectric

against high electric fields by pushing the depletion region away from the insulated gate resulting in better reliability (less probability of dielectric breakdown, no tunnelling through oxide and no hot carrier injection) and better breakdown (ii) reduces the Miller (gate-drain) capacitance by pushing the depletion region in the bulk.

The p+ layer under the gate can be connected to source (terminal 1) or a further control terminal. If connected to the source terminal it is very effective in pushing the field away from the dielectric and changing the CGD capacitance into CDS. However it is not straightforward to form this layer in the first place and connect it to source. If connected to ground or a negative voltage it can block the voltage in the off-state. The distance between adjacent p+ layers needs to be carefully optimised to deliver a high breakdown voltage. Note however, that the p+ introduces an additional JFET parasitic effect in the on-state, obstructing the current to flow between the depletion regions. This effect increases the on-state resistance of the device [25%]

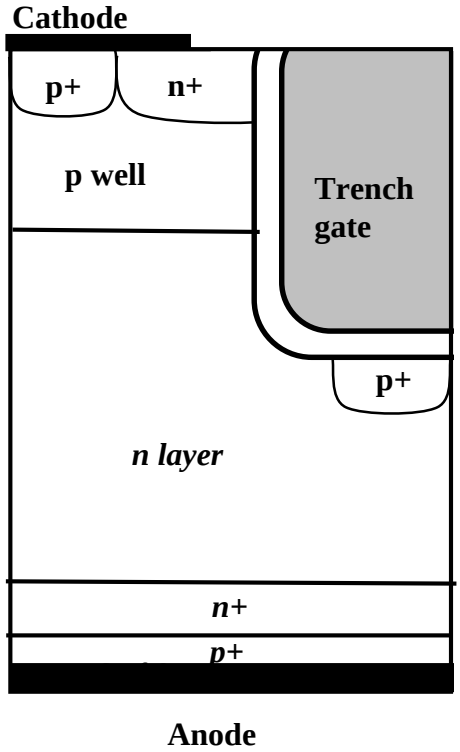
(c) Advantages:

1. The p+ layer helps protecting the trench against reliability and cuts the Miller capacitance
2. If connected to a control terminal, the p+ layer can provide the blocking action via the reverse-biased p+/n layer junction. If connected to a positive potential, (i) the JFET depletion region can be eliminated and (ii) holes can be injected for conductivity modulation. Both these effects lead to lower on-state resistance.

Disadvantages:

1. Making the p+ under the trench is a difficult and expensive process
2. Contacting p+ to source or another terminal requires additional complexity in both making the device and driving the device while in operation. [20%]

(d)



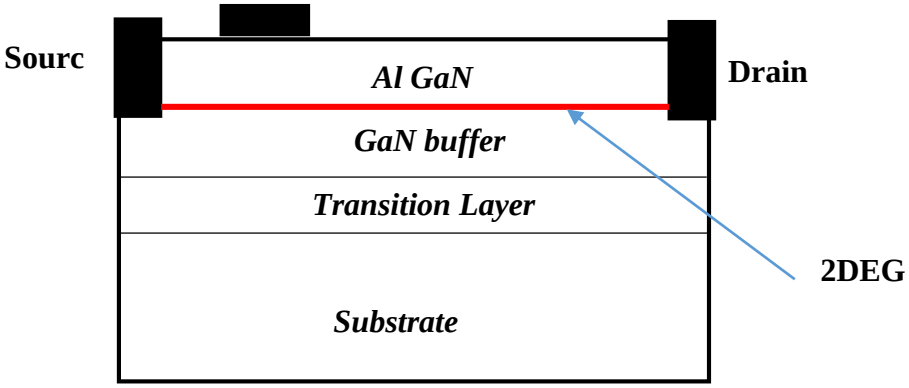
The device in Fig. 2 can have an additional hole injector placed in contact with the high voltage terminal (now named Anode). The hole injector establishes bipolar conduction in the n-layer and hence conductivity modulation.

Challenges: (i) SiC wafers have more defects than Silicon wafers - ensuring high and reproducible lifetime in the n layer is a challenge. (ii) forming the p+/n+ layer combination on the anode side is technologically challenging

Benefits: For very high voltage ratings >10kV, the n layer doping must be low and conductivity modulation helps to reduce its on-state resistance and on-state losses.

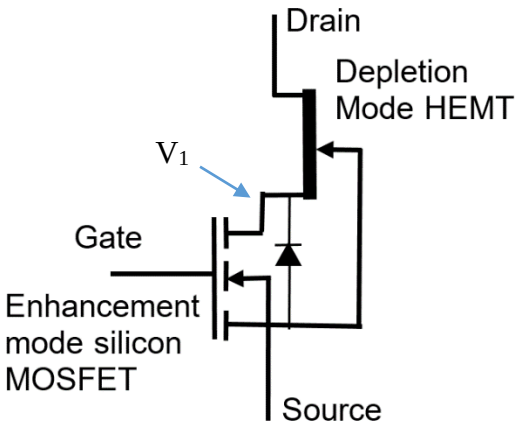
Drawbacks: (i) The device suffers from a large anode junction voltage drop (because of the wide bandgap of Silicon Carbide) ~ 2.3 V and this is the reason the device cannot bit a SiC MOSFET below 10kV. (ii) The device has higher turn-off losses than a unipolar device because of the plasma stored during on-state. [25%]

4. (a) The device is based on a Two Dimensional Electron gas (2DEG) formed between a GaN buffer and an AlGaN layer placed on top. The current flows from the source to the drain through the 2DEG layer. The gate modulates the flow of the electron current through the 2DEG. Because the gate is based on a Schottky metal placed directly on the AlGaN, the device is normally-on with a negative threshold voltage. In the on-state, the resistance of the device is proportional with the length of the 2DEG channel from source to drain and inverse proportional to the conductivity of the 2DEG. In the off-state the device can block high voltages applied to the drain, by depleting 2DEG. The depletion starts from the Schottky contact and moving laterally towards the drain and vertically towards the substrate



[20%]

(b)



The device is based on a series connection of a low-voltage Si MOSFET and a high voltage HEMT. The source of the HEMT is connected to the drain of the Si MOSFET. The potential of this node is shown in picture as V_1. Note that the gate of the HEMT sits at low potential (ground) and is connected to the source of the Si device.

In the off-state, while blocking the voltage, the drain of the MOFET is raised (V_1 is raised) giving a negative Vgs on the HEMT as the gate of the HEMT is connected to ground (source of Si MOSFET). Vgs of the HEMT is less than the Vth of the HEMT. In this way both devices are blocking the voltage with the larger portion being blocked by the HEMT.

In the on-state, V1 is slightly positive but Vgs of the HEMT > Vth of the HEMT as this is a depletion MOSFET. In this mode the on-state resistance is given the series resistance of the Si MOSFET and that of the GaN HEMT. Note that the MOSFET is rated for low voltages and its resistance is relatively

small in the on-state. The turn-on and turn-off are governed by the signal applied to the gate of the Si MOSFET. When the channel of the Enhancement mode silicon MOSFET is cut-off (its own gate-source voltage is smaller than its positive threshold voltage) the entire current through the CASCODE device is cut-off.

During the turn-on of the MOFET the V_1 is lowered allowing the opening of the depletion mode MOSFET and the current starts to flow through the two devices in series [30%]

(c) Benefits: (i) The control terminal is the same as the gate terminal of the Si MOSFET. It is a normally-off control with positive threshold voltage (Vth ~2 to 3V) which can easily adjusted. By contrast the p-GaN has lower threshold voltage (~15,V) and cannot be easily adjusted. The maximum gate voltage depends on the gate dielectric and can be easily 20 V, much larger than that of the p-GaN gate (~ 7V)
(ii) The depletion mode HEMT has lower on-state resistance than the enhancement mode HEMT and requires a simpler (and less expensive) process using Schottky metal, rather than p-GaN which uses Magnesium doping.
Drawbacks: (i) There are two components in different technologies and materials to be packaged. The overall chip is more complex, requires bigger package and has higher assembly cost
(ii) The on-state resistance is given by the series resistances of the two components. As GaN technology is evolving, and the GaN specific resistance is cut, the Silicon resistance would start to become important (the Silicon is already optimised to a minimum). The overall specific on-state resistance of the CASCODE is likely to become larger than that of a single enhancement HEMT. [15%]

(d) This is an intrinsic anti-parallel diode which exists in any power MOSFET. It is a bipolar diode (PIN diode) formed between p-well and n- drift layer. When forward biased, it has a 0.7 V junction voltage + the voltage drop across . Overall this diode in series with the 2DEG of the HEMT forms the reverse conduction path of the CASCODE device. It can be used a freewheeling component. The dynamic reverse recovery losses are small as the drift region of the Si MOSFET is short, but not negligible as there is still charge (plasma) stored in this drift region.
[20%]