Solutions 4B2 2022-2023

1 (a)

The properties for Si and GaN are listed below.

Band gap (eV)	1.1	3.4
Relative permittivity	11.9	9.5
Breakdown field (MV/cm)	0.3	3.3
Thermal conductivity (W/K/cm)	1.48	1.3
Mobility (cm2/(Vs)	1350	1200 (bulk) 2000 (for 2DEG)
Saturation velocity (107cm/s)	1	2.5

GaN has > 10x increase in the critical electric field. The drift region can be made > 100x more highly doped and > 10x thinner in GN than in Silicon. If a HEMT is used (as opposed to a vertical GaN), the charge in the 2DEG can reach 1e13 cm-2 and the mobility can further be increased to 2000 Cm2/(Vs). The thinner (smaller) drift region and the high doping or the presence of the 2DEG result in significantly lower on-state losses. This could also result in a smaller chip area which allows smaller capacitances and therefore faster speed. HEMTs are lateral devices. They are commonly made on Silicon substrate and they are popular between 100 V to 700V.

However there are challenges in designing and fabricating HEMTs above 1.2 kV. The drift region increases, making the chip area too large. The epi layer needs to be thinker to support the breakdown between the drain and the substrate, making the process more expensive. At 1.2 kV the vertical SiC power MOSFETs are gaining traction and lateral GaN HEMTs have made very little progress. [30%]

(b) *f= 1/T and varying from 100 kHz to 500 kHz* $D = 50\%$, $t_{on} = DT = \frac{D}{f}$

ON-STATE

$$P_{\mathrm{ON}} = \frac{1}{T}\int_0^{t_{\mathrm{ON}}} \mathrm{V}_{\mathrm{ON}} I_{\mathrm{ON}}\, dt = V_{\mathrm{ON}} I_{\mathrm{ON}} D\ ,$$

P_{ONSJ} *= 3x3x1/2= 4.5W*

P_{ONIGBT} *= 1x3x1/2= 1.5W*

P_{ONGaN}*=2x3x1/2=3W*

TURN – OFF

Delay time: $P = V_{\mathrm{ON}} I_{\mathrm{ON}} t_s f$

P_{dSJ}*= 3x3x0.1x10*$^{-6}$*f = 0.9 x10*$^{-6}$*f*

P_{dIGBT}*= 1x3x0.1x10*$^{-6}$*f =0.3 x10*$^{-6}$*f*

P_{dGaN}*= 2x3x0.01x10*$^{-6}$*f =0.06 x10*$^{-6}$*f*

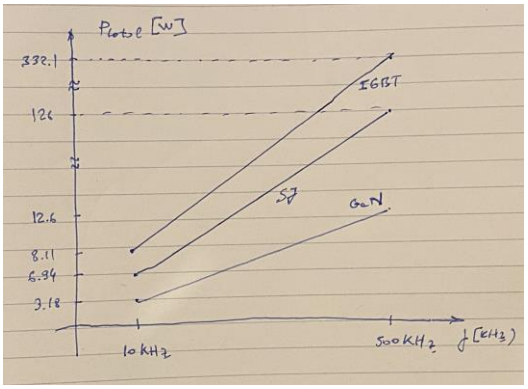
Growth time:

$$P_g = \frac{1}{T}\int_0^{t_g} I_{ON}\left(V_{ON} + \frac{V_{dc} - V_{ON}}{t_g}t\right) = t_g f I_{ON}\left[\frac{V_{dc}}{2} + V_{ON}\right]$$

P_{gSJ}= 0.3x3x203x10^{-6}f = 182.7x10^{-6}f

P_{gIGBT}= 0.3x3x201x10^{-6}f = 180.9x10^{-6}f

P_{gGaN}= 0.0.1x3x202x10^{-6}f = 6.06x10^{-6}f



Fall time :

$$P_f = tf \times f \frac{V_{dc} \times I_{ON}}{2}$$

P_{fSJ}= 0.1x3x200x10^{-6}f = 60x10^{-6}f

P_{fIGBT}= 0.8x3x200x10^{-6}f = 480x10^{-6}f

P_{fGaN}= 0.02x3x200x10^{-6}f = 12x10^{-6}f

Total losses (on-state + delay+turn-off):

$P_{totalSJ}$ =4.5+ 0.9 x10^{-6}f +182.7x10^{-6}f + 60x10^{-6}f = 4.5+243.6 x10^{-6}f

$P_{totalIGBT}$ =1.5+ 0.3 x10^{-6}f +180.9x10^{-6}f + 480x10^{-6}f = 1.5+661.2 x10^{-6}f

$P_{totalGaN}$ =3+ 0.06 x10^{-6}f +6.06x10^{-6}f + 12x10^{-6}f = 3+18.12 x10^{-6}f

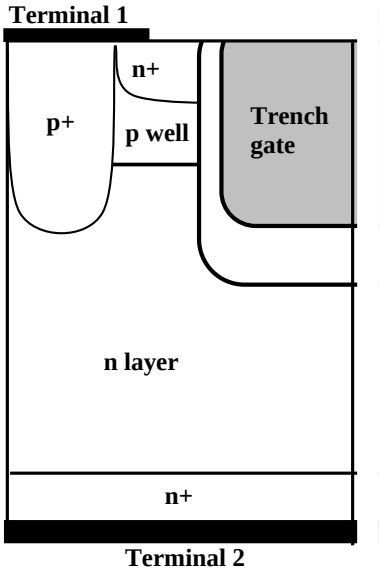
At 10 kHz, $P_{totalSJ}$ =6.94, $P_{totalIGBT}$=8.11 $P_{totalGaN}$=3.18

At 500 kHz $P_{totalSJ}$ =126, $P_{totalIGBT}$=332.1 $P_{totalGaN}$=12.6

GaN is best at all frequencies (10kHz to 500 kHz) . SJ is second best and the IGBT is worst. At high frequencies only GaN can be operated efficiently. In terms of the cost the IGBT is the cheapest followed by the Superjunction and GaN is the most expensive, At very low frequencies the IGBT and the SJ can compete due to cost reduction. [50%]

(c) In the unipolar devices (SJ and GaN) the on-state resistance (on-state voltage) is expected to decrease by ~1.5x from 25C to -55 ºC. This is because the electron mobility increases at lower temperatures. The turn-off losses in unipolar devices are generally unaffected. In the IGBT, it depends if a positive temperature coefficient (NPT) or negative temperature coefficient (PT) design is employed. In any case the voltage drop can increase or decrease by a very small amount (say 0.1 V – 0.3V). The turn-off losses are expected to decrease slightly in the IGBT as there is less plasma present at lower temperatures. In general, the ambient temperature and self-heating can influence the choice of the device, however in this particular case the GaN remains the best due to the very fast switching at all temperatures. [20%]

2.



Terminal 1 – Source, Terminal 2 – Drain. This is a Trench MOSFET type structure with unipolar conduction and controlled through the potential applied to the insulated trench gate.

The device is made in Silicon Carbide which means the drift region is thin and very highly doped. This is advantageous in the on-state, but the field in the drift region is very high putting pressure on the trench oxide.

- The turn-on : Vgs >Vth such that a channel is formed on the side walls of the trench and allowing electrons top flow from the source terminal through the channel formed in the p-well into the n-layer (drift region) and to the n+ contact
- In the on-state, the gate potential remains ON and in the linear region the device behaves as a resistance. The dominant resistances are the channel resistance and the drift resistance. The parasitic JFET resistance can also play a role. The parasitic JFET effect is still present between the deep p+ well and the trench wall.
- In the off-state, the device is blocking the voltage due to the action of the depletion region extending into the n-layer (generated at the reverse biased p-well/n layer junction). In this mode Vgs <Vth
- The turn-off, the channel is stopped by applying a step of Vgs <Vth. The turn-off speed is limited by the internal parasitic capacitances

The thick oxide at the bottom of the trench has a dual purpose (i) it protects the trench corner and the trench bottom as the filed in the oxide is smaller which results in in better reliability (less probability of dielectric breakdown, no tunnelling through oxide and no hot carrier injection) (ii) reduces the Miller (gate-drain) capacitance by increasing the thickness of the dielectric present between the Gate and the drift region.. [30%]

(b) The p+ layer under terminal 1 pushes the electric field away from the corner of the trench and therefore further reduces the field at the trench corner. The deep p+ short also suppresses very efficiently the parasitic npn transistor which can turn on in conditions such as short-circuit.

Note however, that the deep p+ introduces an additional JFET parasitic effect in the on-state, obstructing the current to flow between the depletion regions formed around the deep p+well/n-layer junction and (2) the side of wall of the trench. This effect increases the on-state resistance of the device. [20%]

(c)

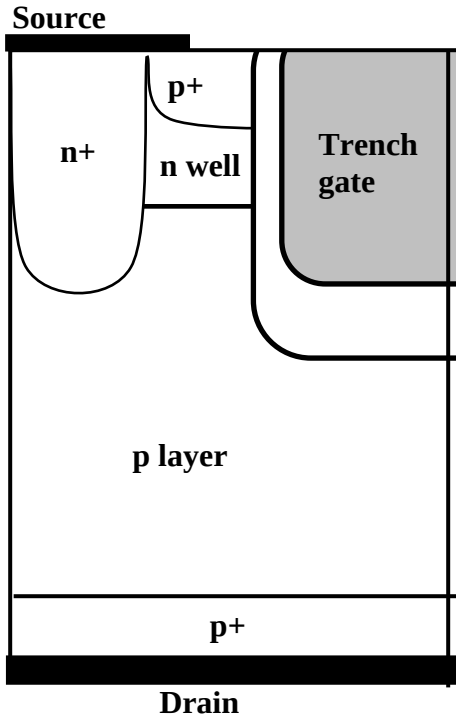
Advantages:

1. The thick oxide reduces the Miller capacitance (allowing for faster dV/dt transients) and results in lower oxide fields (enhanced reliability)
2. The deep p+ layer helps protecting the trench against high fields, hence enhancing reliability, and supresses the npn bipolar transistor,

Disadvantages:

1. Making a deep p+ well in SiC is very difficult as dopants have extremely low diffusion. This requires multiple implants or selective epitaxy which are both challenging and expensive..
2. Depositing or growing a different oxide thickness on the bottom of the trench to that of the side walls is challenging. The relatively low oxide thickness on the side walls is required for a relatively low threshold voltage, and low channel resistance. [25%]

(d)



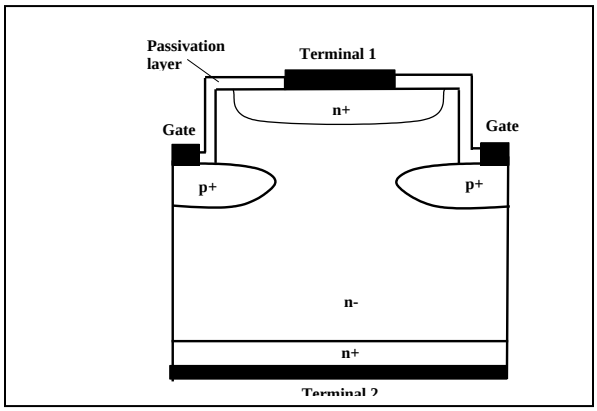
Change pinto n and vice-versa. The device is based on hole conduction rather than electron conduction.

Challenges: p+ wafers and p epi are more expensive and less common. Benefits: Could be used in high side with the gate referred to the upper rail voltage – does not need level shifting to the gate in half bridges. Drawbacks: High cost, low mobility of holes, inefficient. [25%]

3. **(a)** The structure is a JFET type structure in GaN. Terminal 1 is the source of electrons. Terminal 2 is the drain of electrons. It is a junction controllable device and comprises a JFET and a bipolar diode. To obstruct the current flow and turn-off the device, the gate is biased negatively with respect to the cathode to form two depletion regions. When the two depletion regions meet, the current is pinched off, stopping the drift of electrons from Terminal 1 (source) to Terminal 2 (drain).

   Depending on the pitch between the p+ regions, the device can be (i) normally off - if the depletion regions created by the intrinsic potential meet when the gate-source voltage is zero volts, or (ii) normally on - if a negative voltage is needed to extend the depletion regions so that they pinch the current between source and drain. A small pitch between p+ layers results in normally-off behaviour or a relatively large pitch can give a normally on behaviour.

- In the off-state, during the blocking mode, when the drain is biased at high voltage with respect to the source the voltage is supported in the n- drift region. The p+ layers/n – drift junction is reverse biased and the two depletion regions formed from the p+ meet laterally to pinch the current.
- The device is turned on by removing the negative voltage applied to the gate connected to the p+ layers (or applying a slight positive voltage between the gate and the cathode). As result the depletion region around the p+ layers collapses allowing electrons to drift from source to drain.
- The turn-off of the device is achieved by negatively biasing the gate voltage with respect to the source potential. As a result, the depletion regions formed around the p+ layers pinch the electron current flow and consequently the device turns off.



[35%]

(b) Consider the gate voltage range as [v_{gmin}, v_{gmax}]. v_{gmax} cannot be greater than the opening voltage of the p+/n- drift region junction (~ 2.5 V for GaN) as this would result in hole injection from the p+ layer into the n- junction. Due to the low lifetime of carriers in GaN, and the high doping of the n- drift layer (because of the high critical electric field of GaN) this is unlikely to produce significant conductivity modulation to reduce the on-state resistance, but, instead, produce un-necessary plasma which needs to be removed during the turn-off. Additionally a large current needs to be provided by the driver to support the hole current injected from the p+ layer into the n- drift region. To avoid this the maximum voltage applied to this junction (gate-terminal 1 voltage) should be less than ~ 2.5 V (the opening voltage for the p+/- junction in GaN).

V_{gmin} is given by the minimum voltage (negative voltage) that can be applied before the PIN diode between the p+ Gate/n-/n+ Source breaks down. This could be a relatively large negative voltage (e.g. – 40V). [20%]

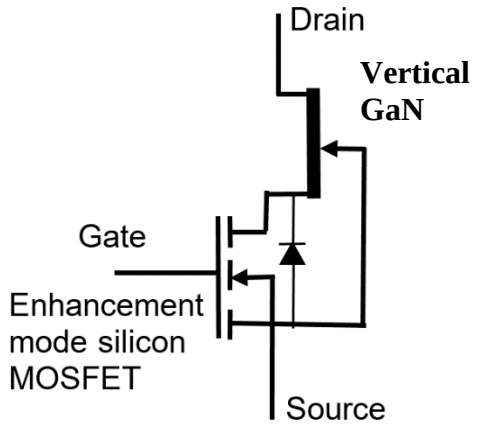
(c)

- Advantage: The device is made in GaN, benefiting from a high critical electric field and therefore (i) very high doping in the drift region and (ii) thin drift region - both of which would result in very low specific on-resistance, significantly lower than that offered by the SJ device.
- Disadvantages: The device has no high impedance control (MOS gate). The device may require negative bias for keeping the device in the off-state, which means more complexity in the drive. [10%]

(d)

- Advantage: GaN has higher mobility and higher critical electric field than SiC both of which means lower specific on-state resistance.
- Disadvantage 1: Vertical GaN technology is considerably less mature than SiC, and therefore more difficult to fabricate and could result in higher cost
- Disadvantage 2: SiC has better thermal conductivity than GaN and therefore the GaN device can yield higher temperatures due to self-heating for the same power applied to the chip (and considering the same package). This could both impact negatively the on-state resistance and the reliability. [10%]

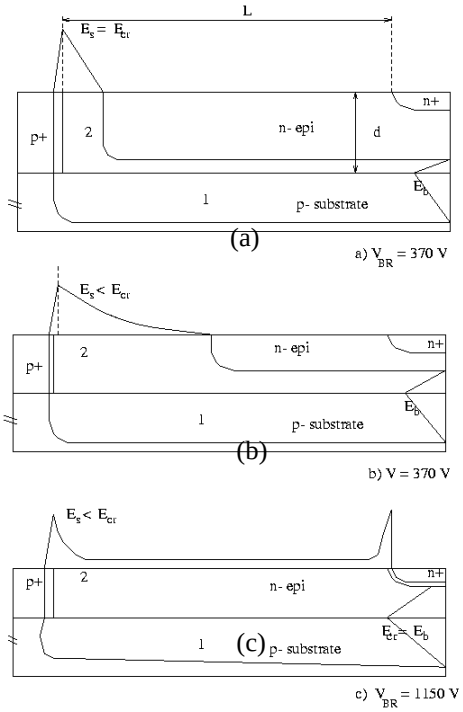
(e)



The vertical GaN JFET could be put in series with a silicon MOSFET. Here it is assumed that the GaN JFET is a normally -on device. The GaN JFET conducts at low negative gate- terminal 1 voltage (e.g. – 2V) but blocks at large negative gate-terminal 1 voltage (e.g. -30 V). The CASCODE delivers a normally-off operation (because of the enhancement Si device) in spite of the GaN JFET having a normally-on behaviour.

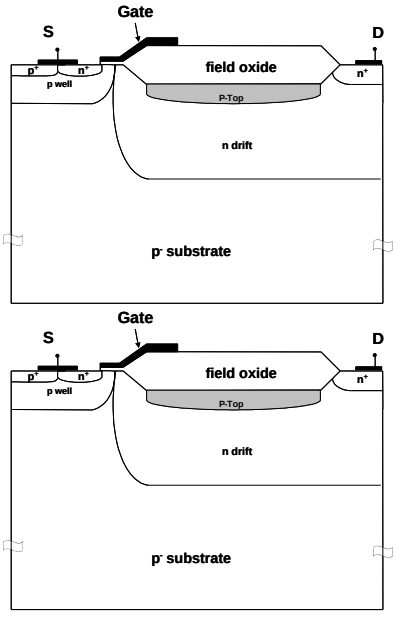
(c) Benefits: (i) The control terminal is the same as the gate terminal of the Si MOSFET. It is a normally-off control with positive threshold voltage (Vth ~2 to 3V) which can easily adjusted.
(ii) The vertical normally-on GaN JFET has lower very low specific on-state resistance (lower than an equivalent normally-off GaN JFET).
Drawback: There are two components in different technologies and materials to be packaged. The overall chip is more complex, requires a larger package and has higher assembly cost. [25%]

4. (a) The RESURF effect exploits the meeting of the depletion layers from the horizontal n-epi/p-substrate junction and the n-epi/p well vertical junction to enhance the growth of the depletion layer at the surface. This can be viewed as a more rapid growth of the depletion region than predicted by the 1-D Poisson equation solution for the vertical n-epi/p well junction. Fig (a) on the right shows no interaction between the two depletion regions. Fig. (b) shows that by reducing the n- drift region the two depletions start interacting and the electric field at the surface is lowered. Fig. (c) shows the depletion region and the optimum surface electric field at breakdown. There are three electric field peaks present (two at the surface and one in the bulk at the n- epi/p- substrate junction.



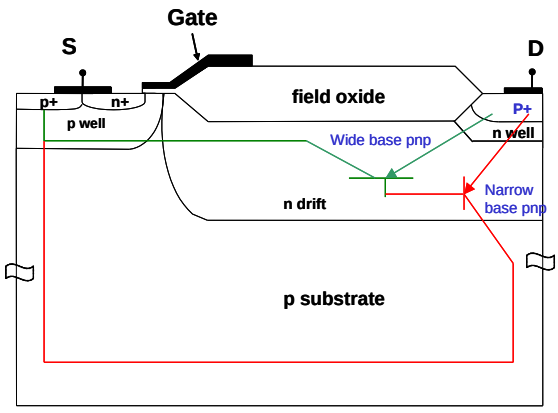
[30%]

(b) The Double RESURF LDMOSFET features a p-top at the surface of the device. This is more highly doped than the n-drift region, but is completely depleted at breakdown. Its presence helps further the advance of the depletion region in the n-drift region. As a result the doping of the n- drift region can be increased (almost by 2X) compared to that of a single RESURF device.



[20%]

(c) LIGBTs. The structure of the LIGBTs is shown on the right. The presence of the two bipolar elements is indicated.



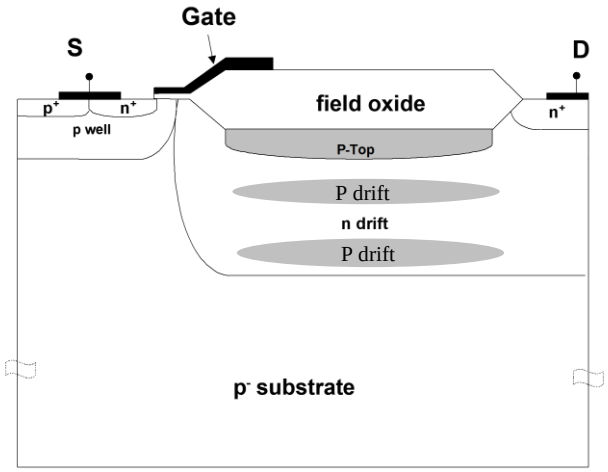
Turn-on: This is similar to the LDMOSFET. The channel induced at the surface of the p well allows flow into the drift region providing that the anode junction is forward biased. The electron current acts as the base current for the pnp transistor leading to injection of holes into the drift region.

On-state: The injection of both holes and electrons into the drift region leads to accumulation of excess mobile carrier charge formed by electrons and holes in equilibrium. As a result the resistance of the drift layer decreases significantly. Note that there are two bipolar transistors (wide-base and narrow base). The narrow base transistor tends to inject plasma deep in the substrate. This transistor is not present in the vertical devices.

Turn-off: The turn-off process is based on sweeping of holes to the cathode short when the depletion advances in the n- drift region from the p well side. Another major turn-off mechanism is via recombination of holes and electrons in the drift region, especially at the anode side where the depletion region takes time to reach. Unfortunately, injection in the on-state does not only occur in the drift region but also in the substrate via the parasitic pnp transistor p+ anode/n-epi/p-substrate. Thus accumulation of parasitic mobile charge occurs deeply in the substrate. This charge has to be removed during turn-off which slows down considerably the turn-off process. Therefore, the turn-off of the LIGBT is generally slow characterized by a specific long tail. As a result the lateral devices can be slower than the vertical devices.

Blocking: This is similar to the LDMOSFET, however in most cases slightly smaller because of the gain of the pnp transistor during avalanche. [30%]

(d) A superjunction in the drift region could be made by adding stripes of p-drift layers between the n-drift layers. These layers are thin and highly doped. In the on-state, the current flows in the n drift stripes between the p layers. Given the high doping of the n drift layers (much higher than in Single and Double RESURF LDMOSFETs), the on-state resistance is decreased.



If charge compensation is achieved, the structure can enhance the breakdown voltage with very low on-state resistance. The electric field at the surface will have almost a rectangular distribution (ideal for power devices). [20%]