Version FU/3

EGT3
ENGINEERING TRIPOS PART IIB

Monday 24 April 2023 2 to 3.40

Module 4B2

POWER MICROELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination room.

Version FU/3

1. (a) Based on the physical properties of Gallium Nitride (GaN) and Silicon, state the advantages of GaN High Electron Mobility Transistors (HEMTs) compared to Silicon Power MOSFETs. Why are there no HEMT products rated above 1.2 kV in the market? [30%]

(b) Three different power devices are to be assessed for an SMPS application: a Silicon Superjunction MOSFET, a Silicon IGBT and a Gallium Nitride HEMT. The typical switching waveforms applicable to all three devices are shown schematically in Fig. 1. The rail voltage V_{dc} = 400V and the on-state current I_{ON} = 3A. The static and dynamic parameters of the three devices are summarised in table 1. Consider that the turn-on and the off-state losses are negligible for all devices. The switching frequency is variable from 10 kHz to 500 kHz with a constant duty cycle of D = 50%.

Table1

Parameter	On-state voltage drop V_{ON} [V]	Turn-off delay time t_s [μs]	Turn-off voltage growth time t_g [μs]	Turn-off current fall time t_f [μs]
Silicon Superjunction MOSFET	3	0.1	0.3	0.1
Silicon IGBT	1	0.1	0.3	0.8
Gallium Nitride HEMT	2	0.01	0.01	0.02

(i) Estimate the total power losses in each of the power devices and sketch a graph of these as a function of frequency. Comment on the efficiency of these devices and the preferred use of one against the others. [50%]

(ii) Assume that the parameters in Table 1 are given at room temperature. How would you expect the parameters in Table 1, and hence the total power losses, to change at sub-zero Celsius temperatures? Will the ambient temperature or self-heating influence the choice of the transistor? [20%]

(cont.

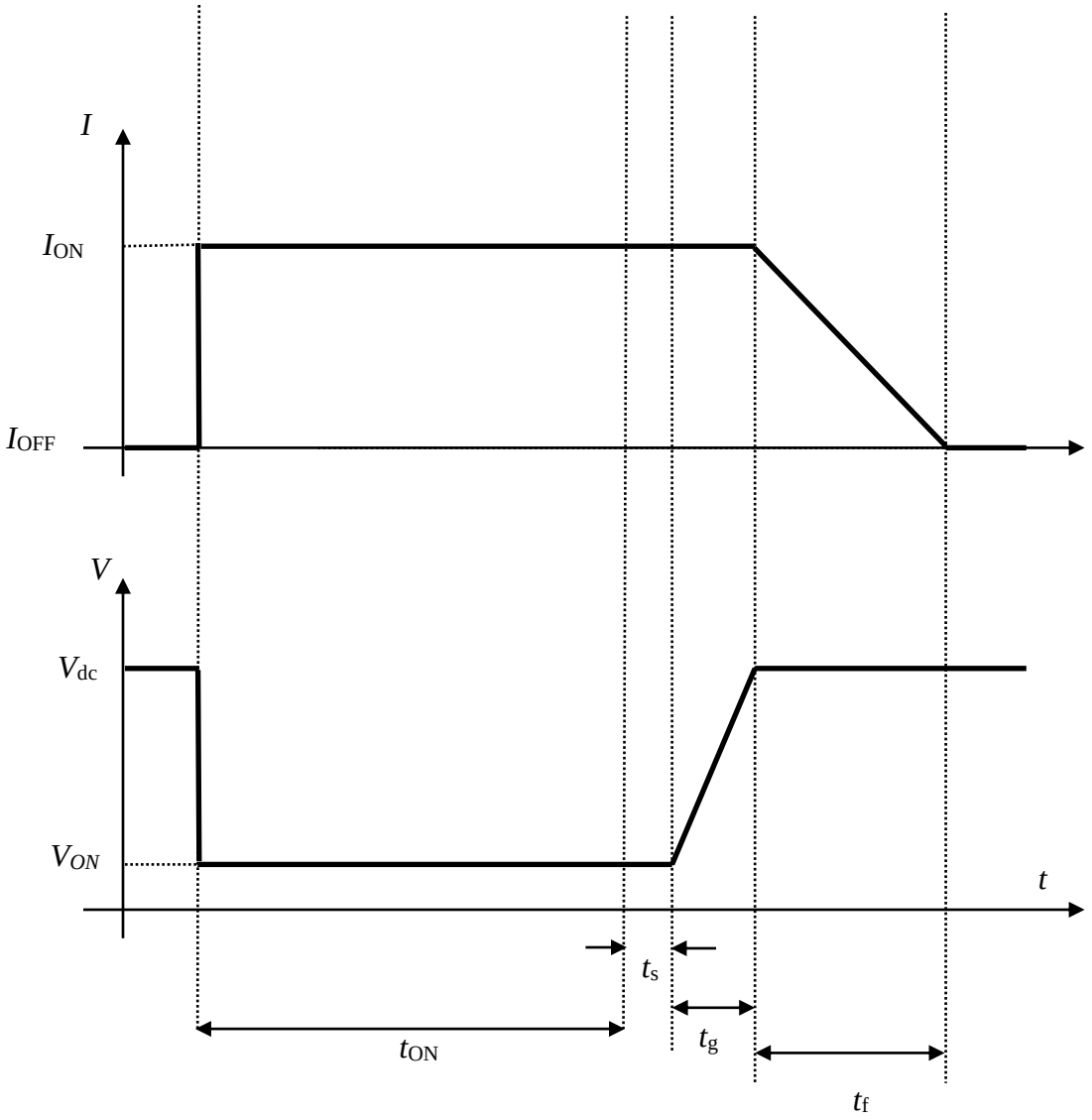

Fig. 1

2 The cell structure in Fig. 2 represents a vertical Silicon Carbide power device. The oxide at the bottom of the trench gate is thicker than that on its side walls.

(a) Explain its operation during on-state, off-state, turn-on and turn-off and emphasize the role of the thicker oxide at the bottom of the trench in both static and dynamic conditions. [30%]

(b) What is the role of the deep p+ layer placed under the Terminal 1? [20%]

(c) Give two advantages and two disadvantages of this device compared to a conventional Silicon Carbide Trench Power MOSFET. [25%]

(d) Modify the device shown in Fig. 2 to operate as a p-type channel Power MOSFET. What are the challenges, the benefits and the drawbacks of making and using a p-type channel Power MOSFET in Silicon Carbide? [25%]

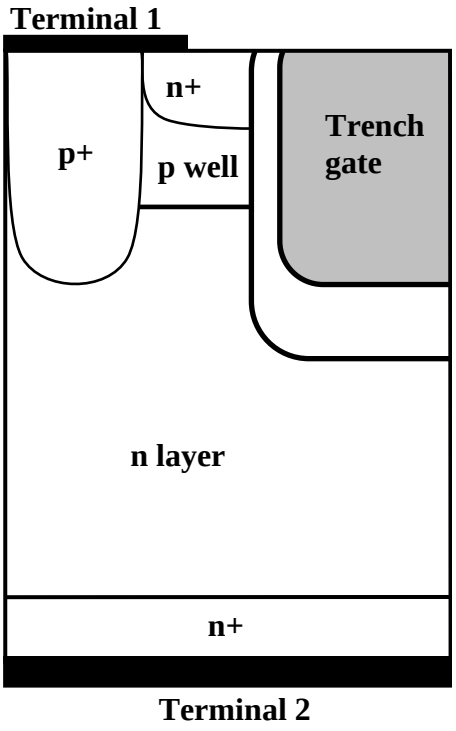

Fig. 2

3. The cell structure in Fig. 3 represents a junction-controlled power device made in vertical Gallium Nitride technology.

(a) Explain its operation during on-state, off-state, turn-on and turn-off. [35%]

(b) What limits the voltage applied between the gate terminal and Terminal 1? [20%]

(c) Give one advantage and one disadvantage of this device compared to a Superjunction Silicon transistor. [10%]

(d) Give one advantage and two disadvantages of this device compared to a similar device made in Silicon Carbide instead of Gallium Nitride. [10%]

(e) Draw schematically how such a device could be used in a CASCODE configuration and give two advantages and one disadvantage of using such a configuration versus an enhancement single-chip power device. [25%]

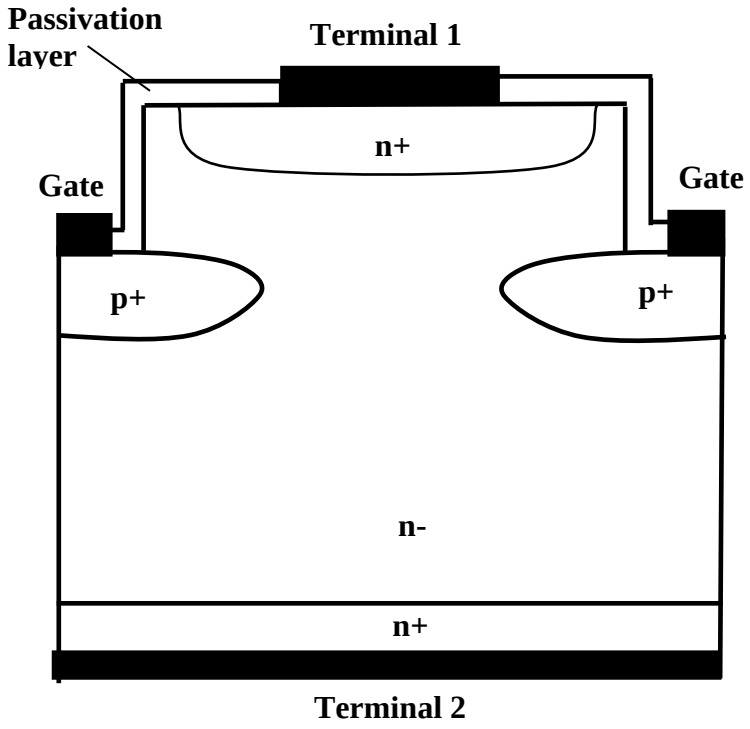

Fig. 3

4. (a) Describe the RESURF effect in a lateral high voltage diode. Show schematically the electric field distribution at the surface of the diode. [30%]

(b) Draw a double RESURF LDMOSFET and explain its advantages compared to a single RESURF LDMOSFET. [20%]

(c) Draw and explain the operation of a lateral Insulated Gate Bipolar Transistor (LIGBT) based on the RESURF effect. Draw an equivalent circuit of the LIGBT and explain its performance when compared to a vertical IGBT. [30%]

(d) Draw and briefly explain the operation of an LDMOSFET featuring a Superjunction in the drift region. [20%]

END OF PAPER