Version FU/3

EGT3
ENGINEERING TRIPOS PART IIB

Monday 22 April 2024 2 to 3.40

Module 4B2

POWER MICROELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination room.

1. (a) Comment on the importance of physical properties, such as dielectric constant, field strength, electron and hole mobilities and thermal conductivity, in making the case for changing silicon power semiconductor devices to wide bandgap power semiconductor devices. [20%]

(b) Figure 1 shows the waveforms of a Silicon-Carbide BJT switch in a simplified resistive switching circuit. The switch operates at a switching frequency f = 20 kHz with a duty cycle D = 50%. The other parameters are: line voltage V_{dc} = 400 V, off-state leakage current I_{OFF} = 1 mA, on-state collector current I_C = 100 A, on-state base current I_B = 1 A, collector-emitter on-state voltage drop V_{CE} = 1 V, base-emitter on-state voltage drop V_{BE} = 2.5 V, turn-on delay time t_d = 0.5 μs, turn-on current rise time t_r = 0.5 μs, turn-off delay time t_s = 1 μs, turn-off current fall time t_f = 1 μs.

(i) Estimate the static, switching and total power losses in the switch. [30%]

(ii) Plot the instantaneous power vs time for one period. [20%]

(iii) Calculate the power loss due to the base current. [10%]

(iv) Explain why the V_{CE} voltage could be below the V_{BE} voltage in a BJT device. [10%]

(v) How would you expect the on-state and transient losses to change if a similarly voltage and current rated Silicon (instead of Silicon-Carbide) BJT is used. [10%]

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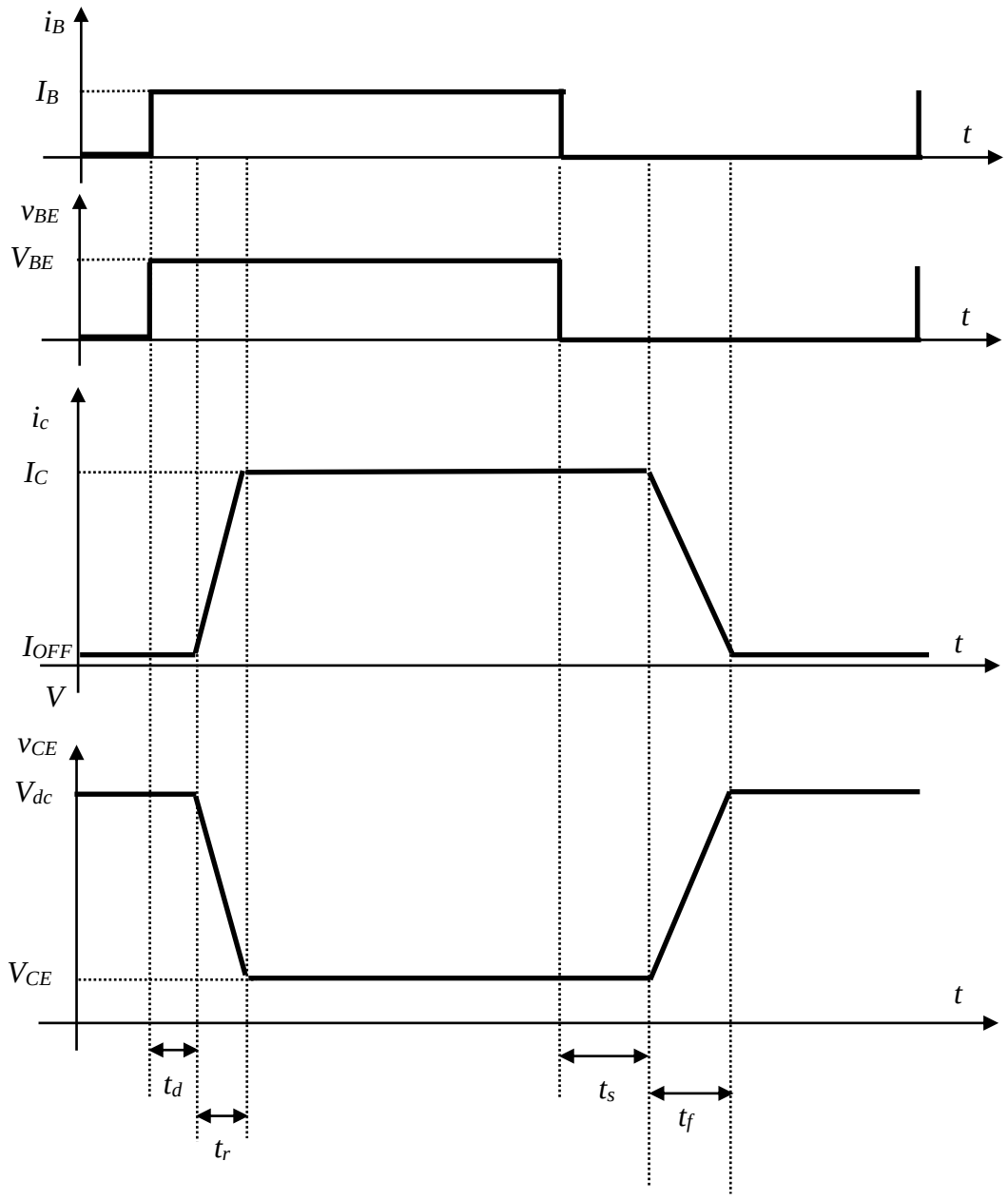

Fig. 1

2 The cell structure in Fig. 2 represents a vertical Silicon Carbide power device. The oxide at the bottom of the trench gate is thicker than that that on its side walls.

(a) Explain its operation during on-state, off-state, turn-on and turn-off and emphasize the role of the thicker oxide at the bottom of the trench in both static and dynamic conditions. [30%]

(b) What is the role of the deep n enhancement layer under the p well ? [20%]

(c) Give two advantages and two disadvantages of this device compared to a conventional Silicon Carbide Trench Power MOSFET. [25%]

(d) Draw a termination structure based on existing layers in the active structure and show schematically the surface electric field distribution in the termination area. [25%]

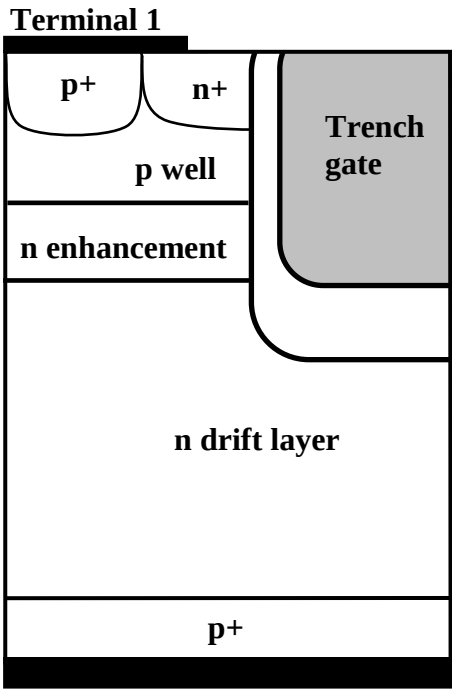

Fig. 2

3. The cell structure in Fig. 3 represents a HEMT in Gallium Nitride technology.

(a) Explain its operation during on-state, off-state, turn-on and turn-off and emphasize the role of the extra p GaN layer at the top of the device. [35%]

(b) What limits the voltage applied between the gate and source terminals? [15%]

(c) Give three advantages and one disadvantage of this device compared to a silicon lateral RESURF MOSFET. [15%]

(d) Explain the formation of the Two Dimensional Electron Gas (2DEG) and give at least two advantages of this conductive layer versus that of a ion-doped layer. [20%]

(e) List at least three materials that can be used for the substrate and state the main advantages and disadvantages compared to each other. [15%]

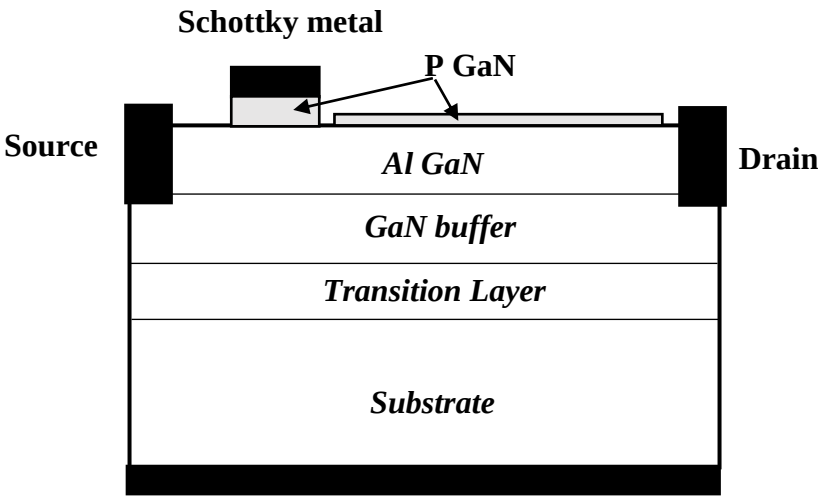

Fig. 3

4. (a) Draw the structure of the Cool MOS and explain its advantage against a Power MOSFET in terms of the trade-off between the specific on-state resistance and the breakdown voltage. [25%]

(b) (i) A Silicon Carbide power MOSFET and a Silicon Cool MOS are to be designed and compared to a reference Silicon power MOSFET. All devices are rated for the same breakdown voltage V_{BR}. Assuming that the critical electric field, E_{cr} remains constant, independent of the doping level, find the optimal doping level and the optimum thickness of the drift region for the Silicon Carbide power MOSFET, as a function of the breakdown voltage, critical electric field and permittivity in Silicon Carbide. [20%]

(ii) What is the optimum thickness of the drift region for the Silicon Cool MOS relative to that of the reference Silicon Power MOSFET? How is this thickness relative to the optimum thickness of the drift region for the Silicon Carbide power MOSFET found in (b) (i)? [25%]

(iii) Assume that the doping levels of the Silicon Cool MOS n-pillar and p-pillar are ten and five times higher than the doping level of the drift region of the reference Silicon power MOSFET respectively. Find the relative change in the specific drift on-state resistance of the Silicon Cool MOS with respect to that of the Silicon Carbide Power MOSFET. Explain the significance of the result found. [30%]

You may assume the following equation in the calculation of the breakdown voltage

$$w = \left[\frac{2\varepsilon_r \varepsilon_0 V}{q} \frac{1}{N_D} \right]^{\frac{1}{2}}$$

where w is the depletion region thickness, N_D is the doping concentration of the drift region, V is the blocking voltage, q is the electronic charge and the other symbols have their usual meaning.

You may also assume that the permittivity of Silicon Carbide is 75% of that of Silicon while the Silicon Carbide critical electric field is a factor of 10 larger than that of Silicon.

END OF PAPER