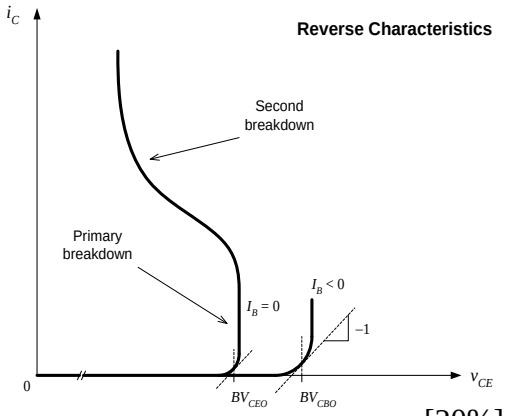
1. (a) ***Second breakdown:*** This is characterized by a snap-back in the breakdown characteristics. The *second breakdown* appears at large currents and results in a fast drop in the collector-emitter voltage. As the current increases, the temperature increases. If the temperature increases the injection is stronger and the current increases again. Hence BJTs suffer from a positive current-temperature feedback. This is known as *thermal runaway (*or the *filamentation effect)*.



(b) (i) $f = \frac{1}{T} = 100\text{kHz} \Rightarrow \text{T} = 10\,\mu s$, [20%]

$D = 50\%$,

$DT = t_{on} + t_r + t_d = 5\mu s \Rightarrow t_{on} = 5 - 0.5 - 0.1 = 4.4\mu s$

$(1-D)T = t_{off} + t_s + t_f = 5\mu s \Rightarrow t_{off} = 5 - 0.5 - 0.3 = 4.2\mu s$

ON -STATE

$$P_{\text{ON}} = \frac{1}{T}\int_0^{t_{\text{ON}}} \text{V}_{\text{CE}} I_{\text{C}}\, dt = V_{\text{CE}} I_{\text{C}} \frac{t_{on}}{T} = 2 \times 100 \times 0.44 = 88W$$

TURN – ON

$$P_d = \frac{1}{T}\int_0^{t_d} V_{dc} I_{OFF}\, dt = t_d\, f I_{OFF} V_{dc} = 2.5mW - (\text{can be neglected})$$

$$P_r = \frac{1}{T}\int_0^{t_r} I_C \frac{t}{t_r}[V_{dc} + (V_{CE} - V_{dc})\frac{t}{t_r}]dt = t_r\, f I_C [\frac{V_{dc}}{2} + \frac{V_{CE} - V_{dc}}{3}] = 9W$$

TURN – OFF

Delay time: $P_s = V_{\text{CE}} I_{\text{C}} t_s f = 10W$

Current fall time:

$P_f = 27W$

OFF –STATE

$$P_{OFF} = V_{dc} I_{OFF} t_{OFF} f = 25mW$$

Total losses (on-state + turn-on + turn-off):

P total= 88+9+37= 134W

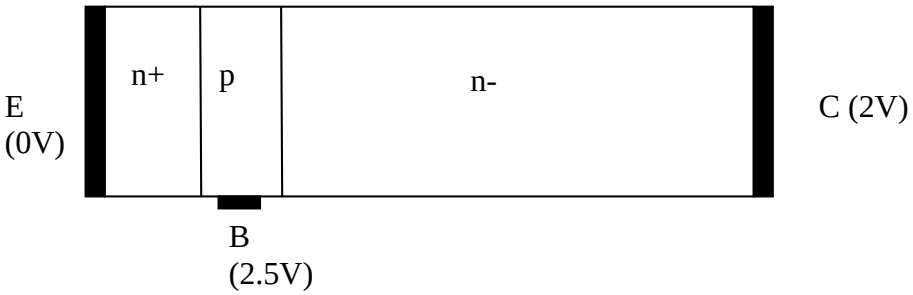
[40%]

(ii) The power loss due to the base current can be calculated as:

$$P_B = V_{BE} I_B D = 2.5W$$

[10%]

(iii) The structure is shown schematically below:



The device is made of a wide bandgap material – Silicon Carbide. This is why V_{BE} is 2.5 V (in Silicon is normally around 0.7V). The base collector junction is also forward-biased (just below 2.5V) and the 2V on-state voltage is mainly dropped across the collector region (as the base-emitter potential drop is almost cancelled out by the base-collector potential drop) . This region is relatively thick to withstand a large breakdown. In this case the breakdown voltage must be well in excess of the line voltage. The device operates in hard saturation during on-state to give a minimum voltage drop across the CE terminals.

[20%]

(iv) The current gain is simply: This is significantly larger than in silicon devices which have a current of typically under 10 for high voltage devices (e.g. 600V). The reason is that the n- drift region (the collector region) is significantly thicker in silicon, decreasing the gain. The base in SiC can also be made thinner and more highly doped to avoid punch-through but without the risk of avalanche as the critical electric field in SiC is ~ 10 times higher than that in Silicon

[10%]

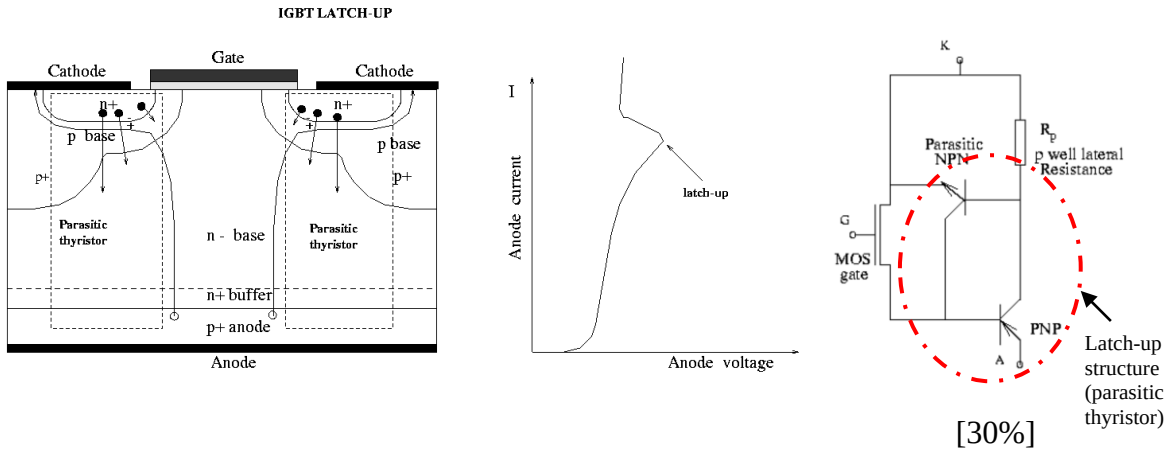
2. (a) The IGBT has a parasitic thyristor formed between the n+ cathode, p well, n- base and p+ anode. To avoid the latch-up of this thyristor, the turn-on of the upper npn transistor must be suppressed. For that the lateral resistance of the p well should be kept as small as possible to avoid the turn-on of the emitter/base junction formed between the n+ cathode and the p base. This is accomplished by :

(a) introducing a deep p+ well diffusion short-circuited to the n+ cathode diffusion through a metal layer. The effect of this is to reduce the resistance of the p well lateral diffusion which lowers the voltage drop across the emitter/base junction

(b) reducing the length of the n+ (by for example using a trench gate structure which cuts the n+ diffusion).

(c) lowering the junction temperature (as the latch-up is exacerbated at higher temperatures)

When the hole current under the n+ cathode develops 0.7 V across the p well lateral resistance, the emitter junction of the npn transistor (i.e. cathode junction) becomes forward biased and the npn transistor turns on. This is followed by injection of electrons straight from the n+ cathode (which becomes an emitter) to the n- drift region (which acts as a collector). The npn together with the pnp will now form a thyristor feedback and the current can no longer be controlled by the gate. Moreover the IGBT in this condition cannot be turned-off. The latch-up can be prevented by lowering the lateral resistance of the p well, lowering the gain of the pnp transistor, or lowering the operating junction temperature. The latter is because the npn transistor can be more easily turned on at higher temperatures. The IGBT structure showing the electron injection straight from the cathode during latch-up, the signature of the latch-up and the equivalent circuit to study the latch-up are shown in the figure below.



[30%]

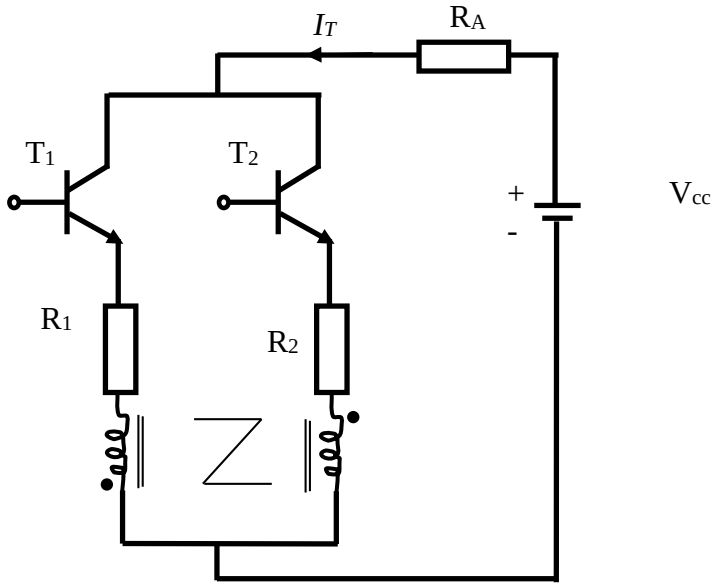
(b) (i) The resistors R_1 and R_2 introduce a negative feedback which helps the equal sharing of the currents in the two BJTs in static conditions. There are two main contributions to this negative feedback:

(1) Let us assume that the current in T_1 is higher than in T_2 (imbalance between the two BJTs). Then the voltage drop across R_1, R_1I_1 is increased. Since $V_{CE1} + R_1I_1 = V_{CE2} + R_2I_2$ = const, then V_{CE1} must go down. Given the output characteristics of the BJT, then the current I_1 must go down (in the saturation region of the BJT) –negative feedback

(2) If the two bases of T_1 and T_2 are connected together, then an increase in the current I_1 results in a higher emitter potential and hence a lower V_{BE} (as V_B is assumed to be at a constant potential). This results in lowering the base current injected in T1 and as a consequence a lower I_1 – negative feedback

[20%]

(ii) The dynamic sharing can be accomplished by connecting some small serial inductors in series with the resistors. If the current rises quickly, then *L(di/dt)*, the voltage drop on the inductor increases and hence VDS is forced to decrease (similarly to point (i)). Another solution is to use couple inductors as shown in the next figure. In this case an *L(di/dt)* increase in one of the inductor, would result in a corresponding voltage of opposite polarity induced across the other inductor. As a result the other inductor will take more current – thus rebalancing the current through the two BJTs, The problem with the inductors is that they can generate spikes and can be expansive and bulky.



[20%]

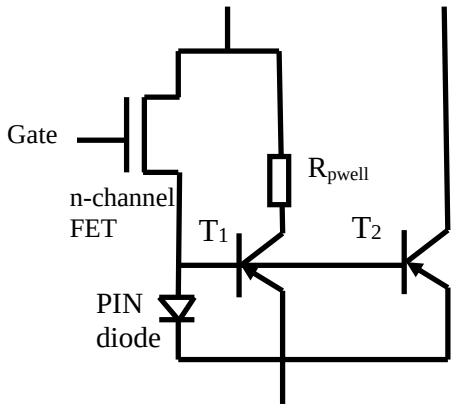
(iii) Assume V_{BE2}= *0.7 V for silicon.*
(1) V_{B1}- V_{BE1} = R_1I_1 *from this* I_1= *(2-0.7)/0.5=**2.6 A***
(2) V_{B2}- V_{BE2} = R_2I_2 *from this* I_2= *(2-0.7)/1=**1.3 A***

The sum of the two anode currents, I_1 and I_2 in the BJTs is equal to the total current I_T.
(3) I_T=I_1+I_2=*3.9A. The sharing is 2.6/3.9=**66.67%** through T1; 1.3/3.9=**33.33%** through T2*
(4) V_{CE1}+ R_1I_1 + R_AI_T= V_{CE2} +R_2I_2 + R_AI_T = V_{CC} *from this:*
V_{CE1}= *250 – 0.5·2.6 - 63·3.9=**3 V*** *and* V_{CE2}= *250 – 1·1.3 - 63·3.9=**3V*** [30%]

3. (a) The structure is a 4-terminal variant of an IGBT with an extra hole collector (HC) terminal. Terminal 1 is the cathode (similar to that of a classical IGBT). Terminal 2 is the hole collector (HC) and Terminal 3 is the anode. Terminal 2 – HC also controls the p+/n-drift junction in a similar way to that of a JFET. To obstruct the current flow and turn-off the device, the HC can be biased negatively with respect to the cathode to form two depletion regions to obstruct the current similar to the way the JFET operates). In addition it will extract faster holes from the drift region.

- In the off-state, during the blocking mode, when the anode (Terminal 3) is biased at high voltage with respect to the cathode (Terminal 1) and Terminal 2, and the gate potential is grounded (no channel in the p-well formed) the voltage is supported in the n- drift region. The p+ layer (HC)/n –drift junction is reverse biased and the p-well/n-drift region is also reverse biased.
- The device is turned on in a similar way to an IGBT, by applying a positive potential to the gate and forming a channel at the surface of the p-well. This will enable electrons to flow from the n+ layer (connected to the cathode) through the channel into the drift region. The HC terminal should be either floating or connected to 0 V (but not connected to a negative potential).
- In the on-state the device is similar to an IGBT with hole injection from the p+ anode (Terminal 3) and electron injection from the channel and accumulation layer. The holes are collected by the p-well and p+ into Terminal 1. If the HC terminal 2 is connected to the ground this will also collect holes. As a result of this extra collection of holes, the electron injection would be weaker and the conductivity modulation at the cathode side of the drift region will reduce. This has an impact on increasing the on-state voltage drop. If the HC terminal 2 is floating in the on-state, this would reduce the on-state voltage drop and the device would be equivalent to an IGBT (although the current will be slightly obstructed by the presence of the two p+ layers).
- The turn-off of the device is achieved in a similar way to an IGBT by extracting holes during the expansion of the depletion region. The presence of the P+ HC layer greatly enhances the collection of holes making the device significantly faster to turn-off. This would result in lower turn-off losses. To further enhance the collection of holes and therefore the turn-off process and, the HC Terminal 2 could be connected to a negative voltage. This would result in an extended depletion region and a preferred path for the holes collection. [40%]

(b)



- T1 is the classical pnp transistor formed between the p+ anode/n-drift region/pwell
- T2 is a pnp transistor formed between p+anode/n-drift region/p+HC layer.
- The PIN diode is formed between the p+anode/n-drift region/n+ accumulation layer

(c) [30%]

- Advantage: The device has an extra path to collect the holes. This results in a faster turn-off compared to a classical IGBT. When the HC terminal is negatively biased an extra-depletion region is built which allows for faster hole extraction and lower capacitances. Both these features result in lower turn-off losses.
- Disadvantages: (i) The device has 4 terminals and it is therefore difficult to drive. In addition, to form the recessed gate and the extra terminal the device requires extra processing steps and hence higher cost. (ii) The device has higher on-state voltage drop (higher on-state losses) as the hole collection results in weaker conductivity modulation at the cathode side of the drift region (less PIN diode effect).

[15%]

(d)

- Changing the p+ with n+ has an immediate impact in the blocking mode. The device is no longer able to block the forward voltage. As the Anode voltage is increased and the Terminal 2 is connected to ground, the PIN diode formed between the P+ anode/n-drift region/ n+ Terminal 2 region will be forward biased. The device has only reverse blocking ability when the surface terminals are all at high voltage and the anode terminal is grounded.
- In the on-state the device will benefit from the extra PIN diode created (as described above) which will lead to very low on-state voltage drop and low power losses. However the device cannot be described as an efficient switch as the blocking ability (off-state) is lost.

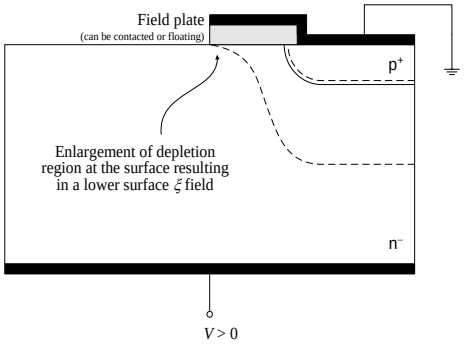
[15%]

4. (a) **Curvature effect**

The shape of the junction which supports the voltage plays an important role in 'field crowding'. The higher the radius of a cylindrical or spherical junction the closer the breakdown is to that of an ideal parallel-plane junction. However, in most microelectronics processes the junction depth is limited to a couple of microns up to maximum 10-15 microns. The curvature effect can be reduced in multiple cell power devices such as MOSFETs or IGBTs by placing the cells (with multiple junctions) close together to simulate almost a 'continuous junction'. By solving Poisson equation for a cylindrical junction one can show that the maximum electric field for the same reverse voltage, increases significantly compared to that in a planar junction.

Edge breakdown

Placing cells very close together has only limited value because at the edge there is always a last cell left 'unprotected'. Premature edge breakdown is a very common effect in power devices. The field plate technique uses a metal layer as shown below. This enhances the effective radius of the junction.



An alternative solution is the floating field ring technique. This is based on distributing the field between highly doped p+ floating field rings to alleviate the edge effect.

A similar result can be obtained with the junction termination extension. This is based on having regions of lowly doped p- layers to spread out uniformly the electric field at the edge of the device. The p- layers have to be depleted at breakdown. [30%]

(b) The field rings that are closer to the active area have a smaller equivalent radius of a spherical (or cylindrical) junction when compared to the field rings that are farther away from the active area. Therefore to avoid high electric fields next to the active area, the inner rings should have a smaller distance between them. Hence they absorb a smaller voltage between them compared to the outer rings. A good optimisation is when all the electric field peaks between the rings are equal at breakdown so the device theoretically breaks in all points at the same time. This would lead to the maximum efficiency of breakdown per unit area. For this the distance between the rings should be increased gradually from the first ring (i.e. the ring that is the closest to the active cell) to the last ring (the farthest from the active cell).

[20%]

(c)

- Increasing the p-well doping leads to a reduced latch-up effect. This is because the hole current flows through this region as it is collected effectively by the cathode short.
- An enhanced p-well doping increases the threshold voltage and therefore increases the on-state resistance.
- Reducing the p-well reduces the threshold voltage, but under a certain level the device becomes affected by noise.
- Reducing the p-well doping can lead to punch-through (in the off-state blocking mode) which in turn results in premature breakdown. This is because at low p-well doping levels, the electric field developed across the p-well/n- drift region junction can reach the cathode junction. [25%]

(d)

- Increasing the p-anode doping leads to an increased hole injection from the anode side of the device which results in enhanced plasma (excess carrier charge) and therefore reduced on-state voltage drop. This is advantageous for reducing the on-state losses. However this also results in more plasma forming in the n-drift region, especially at the anode side of the drift region which results in a slower turn-off process and therefore higher turn-off losses. This could reduce the frequency of operation for the IGBT. Similarly to obtain a fast IGBT, one would reduce the p-anode doping while to compensate for the poorer on-state performance one could increase the PIN diode effect by placing an n-injector near the cathode side of the drift region
- Reducing the p-anode doping could result in poor ohmic contact to the back side electrode (anode terminal). This could result in a Schottky type contact which would severely damage the on-state ability of the device.

[25%]