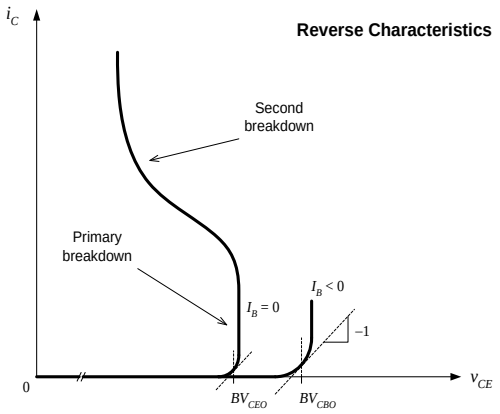
Crib 4B2 – 2021

1. (a) ***BV_{CB0}*** is the breakdown voltage between collector and base when the emitter is floating. This is similar to that of a PT diode and is given by avalanche at the p-base/n0 collector junction.



BV_{CE0} is the breakdown volatge between the collector and emitter when the base is floating. If the base is however in open circuit, the voltage capability of the transistor will be reduced. This is because the avalanche is enhanced by the transistor action (gain). In other words, the high current gain of the BJT leads to the formation of extra pairs of electrons and holes which speed up the process of avalanche. In this case the effective critical electric field at which avalanche takes place is smaller and hence breakdown ocuurs at a lower reverse-bias. The breakdown notation in this case is BV_{CE0}

Second breakdown: This is characterized by a snap-back in the breakdown characteristics. The *second breakdown* appears at large currents and results in a fast drop in the collector-emitter voltage. As the current increases, the temperature increases. If the temperature increases the injection is stronger (and the conductivity of the drift region starts increasing) and the current increases again. Hence BJTs suffer from a positive current-temperature feedback. This is known as *thermal runaway (*or the *filamentation effect)*. The second breakdown does not occur in MOSFETs as there is no conductivity modulation and MOSFETs have positive temperature coefficient. IGBTs also have very low power gains and therefore not enough positive feedback to produce second breakdown.

[20%]

(b) (i) $f = \frac{1}{T} = 100\text{kHz} \Rightarrow \text{T} = 10\ \mu s$, $D = 50\%$,

$DT = t_{on} + t_r + t_d = 5\mu s \Rightarrow t_{on} = 5 - 0.5 - 0.1 = 4.4\mu s$

$(1-D)T = t_{off} + t_s + t_f = 5\mu s \Rightarrow t_{off} = 5 - 0.5 - 0.3 = 4.2\mu s$

ON -STATE

$$P_{\text{ON}} = \frac{1}{T}\int_0^{t_{\text{ON}}} \text{V}_{\text{CE}} I_{\text{C}} dt = V_{\text{CE}} I_{\text{C}} \frac{t_{on}}{T} = 2 \times 100 \times 0.44 = 88W$$

TURN – ON

$$P_d = \frac{1}{T}\int_0^{t_d} V_{dc} I_{OFF}\, dt = t_d\, fI_{OFF} V_{dc} = 12.5mW - (\text{can be neglected})$$

$$P_r = \frac{1}{T}\int_0^{t_r} I_C \frac{t}{t_r}[V_{dc} + (V_{CE} - V_{dc})\frac{t}{t_r}]dt = t_r\, fI_C[\frac{V_{dc}}{2} + \frac{V_{CE} - V_{dc}}{3}] =$$ 9W

TURN – OFF

Delay time: $P_s = V_{CE} I_C t_s f = 10W$

Current fall time:

$$P_f = \frac{1}{T}\int_0^{t_f} I_C\left(\frac{t}{tf}\right)[V_{dc}\frac{t}{tf}dt = t_f\, fl_C \frac{V_{dc}}{6} = \ 25W$$ (neglecting V_{CE} or 27 W without neglecting)

OFF –STATE

$P_{OFF} = V_{dc} I_{OFF} t_{OFF} f = 105mW$

Total losses (on-state + turn-on + turn-off):

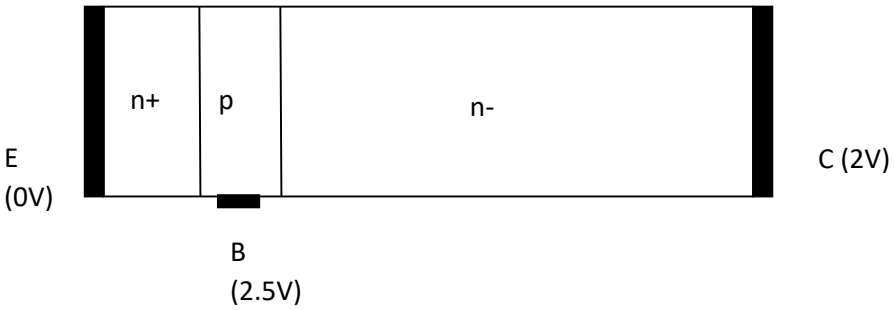
P total= 88+9+ 35W= 132 W (134W if V_{CE} is not neglected in the fall time turn-off losses_

[30%]

(ii) The power loss due to the base current can be calculated as:

$P_B = V_{BE} I_B D + D R_B I_B^2$ = 2.5W + 2W = 4.5W. [10%]

(iii) The structure is shown schematically below:



The device is made of a wide bandgap material – Silicon Carbide. This is why V_{BE} is 2.5 V (in Silicon is normally around 0.7V). The base collector junction is also forward-biased (just below 2.5V) and the 2V on-state voltage is mainly dropped across the collector region (as the base-emitter potential drop is almost cancelled out by the base-collector potential drop) . This region is relatively thick to withstand a large breakdown. In this case the breakdown voltage must be well in excess of the line voltage. The device operates in hard saturation during on-state to give a minimum voltage drop across the CE terminals. [10%]

(iv) The current gain in SiC BJTs - in the example above I_C/I_B= 50 - is significantly larger than in silicon devices which have a current gain of typically under 10 for high voltage devices (e.g. 600V). The reason for that is that the n- drift region (the collector region) is significantly thicker in silicon, decreasing the gain. The base in SiC can also be made thinner and more highly doped to avoid

punch-through but without the risk of avalanche as the critical electric field in SiC is ~ 10 times higher than that in Silicon [10%]

(v)SiC BJTS can operate at higher frequencies as their drift region (collector) is significantly smaller than that of an equivalent silicon BJT. This means that the depletion region is able to clear the charge faster and the device can have a much faster turn-off. High voltage silicon BJTs tend to operate below 10 kHz while SiC BJTs can operate at frequencies as high as 100 kHz. [10%]

(vi) The bandgap of SiC (3.3 eV) is about 3x higher than that of Si. Hence the intrinsic junction voltage for flat bands is expected to also be 3x that of silicon. The Si p-n junction voltage is 0.7V. The SiC p-n junction voltage for full injection is around 2.1-2.5V. . [10%]

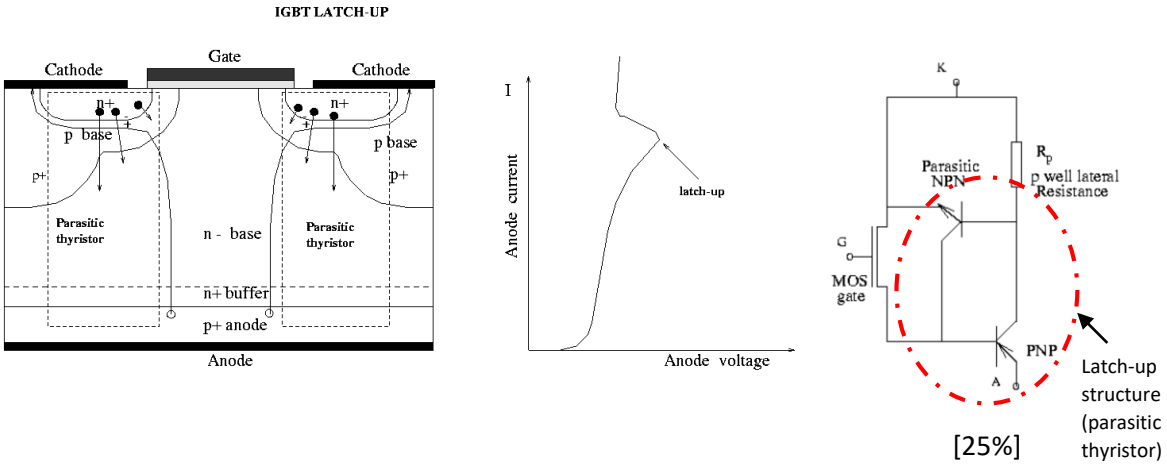
2. (a) The IGBT has a parasitic thyristor formed between the n+ cathode, p well, n- base and p+ anode. To avoid the latch-up of this thyristor, the turn-on of the upper npn transistor must be suppressed. For that the lateral resistance of the p well should be kept as small as possible to avoid the turn-on of the emitter/base junction formed between the n+ cathode and the p base. This is accomplished by :

(a) introducing a deep p+ well diffusion short-circuited to the n+ cathode diffusion through a metal layer. The effect of this is to reduce the resistance of the p well lateral diffusion which lowers the voltage drop across the emitter/base junction

(b) reducing the length of the n+ (by for example using a trench gate structure which cuts the n+ diffusion).

(c) lowering the junction temperature (as the latch-up is exacerbated at higher temperatures)

When the hole current under the n+ cathode develops 0.7 V across the p well lateral resistance, the emitter junction of the npn transistor (i.e. cathode junction) becomes forward biased and the npn transistor turns on. This is followed by injection of electrons straight from the n+ cathode (which becomes an emitter) to the n- drift region (which acts as a collector). The npn together with the pnp will now form a thyristor feedback and the current can no longer be controlled by the gate. Moreover the IGBT in this condition cannot be turned-off. The IGBT structure showing the electron injection straight from the cathode during latch-up, the signature of the latch-up and the equivalent circuit to study the latch-up are shown in the figure below.



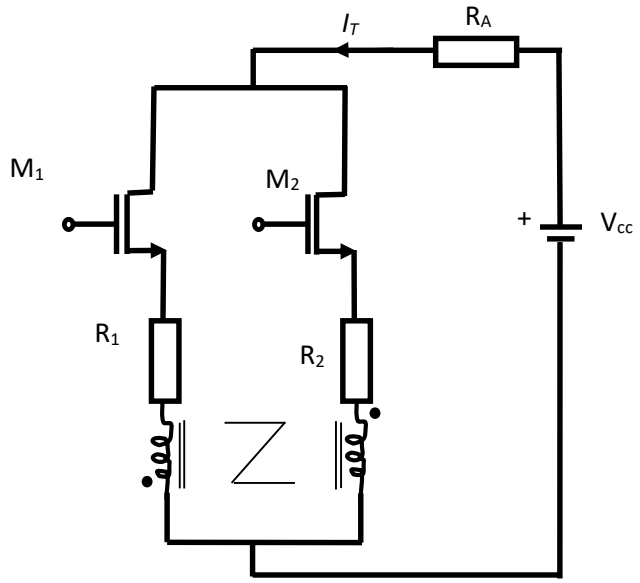
[25%]

(b) (i) The resistors R_1 and R_2 introduce a negative feedback which helps the equal sharing of the currents in the two MOSFETs in static conditions. There are two main contributions to this negative feedback:

(1) Let us assume that the current in M_1 is higher than in M_2 (imbalance between the two MOSFETs). Then the voltage drop across R_1, R_1I_1 is increased. Since $V_{DS1} + R_1I_1 = V_{DS2} + R_2I_2$ = const, then V_{DS1} must go down. Given the output characteristics of the MOSFET, then the current I_1 must go down (in the linear region of the MOSFET) –negative feedback

(2) If the two gates of M_1 and M_2 are connected together, then an increase in the current I_1 results in a higher source potential and hence a lower V_{GS} (as V_G is assumed to be at a constant potential). This results in lowering I_1 due to the incerase in the channel resistance of the MOSFET– negative feedback

[20%]



(ii) The dynamic sharing can be accomplished by connecting some small serial inductors in series with the resistors. If the current rises quickly, then *L(di/dt)*, the voltage drop on the inductor increases and hence V_{DS} is forced to decrease (similarly to point (i)). Another solution is to use couple inductors as shown in the figure above. In this case an *L(di/dt)* increase in one of the inductor, would result in a corresponding voltage of opposite polarity induced across the other inductor. As a result the other inductor will take more current – thus rebalancing the current through the two MOSFETs. The problem with the inductors is that they can generate spikes and can be expansive and bulky. [25%]

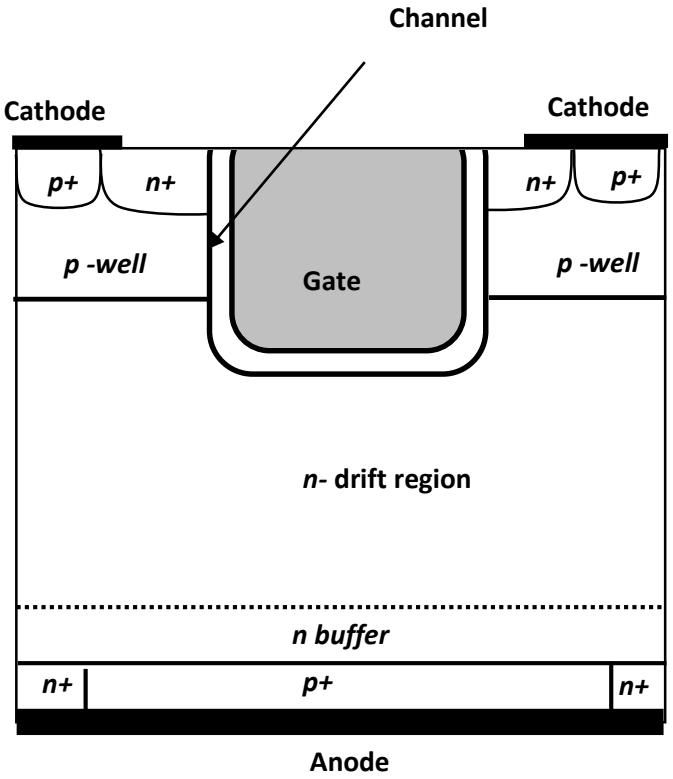
(iii) Both branches have identical transistors and identical resistances. They can be coupled together in a single branche by doubling the area of the MOSFET (or halfing the on-state resistance in the linear region) and by halfing the source resistance (as the two reistors appear now in parallel).

In this case the reistance of the 2xMOSFET is : $900/2(V_G – V_s - V_T)$, where Vs is the source potential. The equivalent reistance in the source (of the single equivalent branch) is 1 ohm - half of that of one of the original branches). The source potential Vs is the product between this equivalent resisance in the source and the current I giving: $Vs = 1 \cdot I$.

Adding the voltages across the 2xMOSFET, the equaivalent source resistance and the R_A gives the rail voltage $V_{CC.}$ Therefore: $I[450/ (11-1 – I) + 49+ 1] = 100$. This means : $450I + 500 I – 50 I^2 = 1000-100 I$.

Rearranging it gives: $50 I^2 - 1050I +1000 = 0$. There are two solutions I=1A or I=20A. Only I=1A has physical meaning. Therefore the total current in the equivalent branch is 1A giving 0.5A in each of the two orginal branches. [30%]

3. 3. (a)

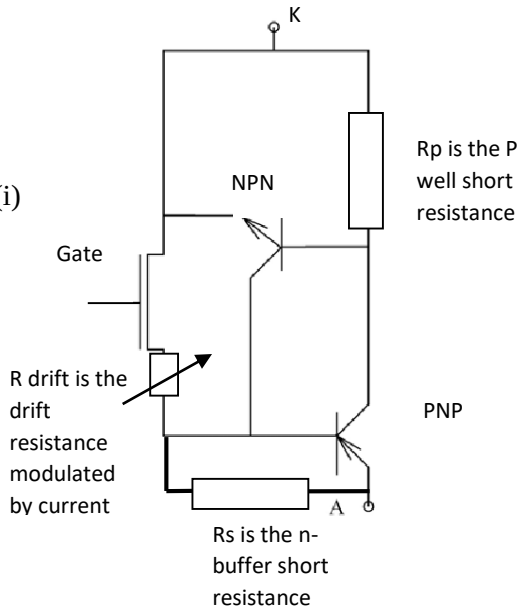


The n+ shorts are connected together with the p+ hole injector to the anode terminal. When the gate is postively biasedwith respect to the cathode and the inversion layer in the p well is formed, electrons can travel from the n+ cathode through the channel (inversion layer) to the n- drift region and are collected by the n+ shorts. In this regime, the transistor operates similarly to a MOSFET based on unipolar conduction. Once the p+/n buffer junction becomes forward biased, holes are injected from the p+ emitter into the n-drift region and via the action of the pnp transistor as well as that of the PIN diode, conductivity modulation (formation of plasma) takes place in the n-drift region resulting in low on-state resistance. The turn-off process is fast, as the pnp transistor is weak (due the shorts) resulting in less plasma accumation in the on-state. Additionally the shorts can collect electrons during the turn-off, further speeding up the turn-off process. The device features a trench gate, which allows for an enhanced PIN diode effect and lower channel resistance. The device is particularly attractive where reverse conduction is needed. This is because the device features an anti-parallel diode formed between the p well (connected via the p+ to the anode of the device), the n- drift and the n+ shorts as the cathode of the anti-paralel diode.

Compared to a standard IGBT, the trench anode shorted device features the n+ shorts. This is good for (i) reverse conducting ability – see above, (Ii) faster switching – see above and (iii) lower off-state leakage current as in the off state the contribution of the bipolar leakage is reduced.

[25%]

(b) (i)



[20%]

(ii) Intially the current is formed by electrons only and flows through the channel of the MOSFET, the drift resistance wihich is conductivity modulated by the current (see figure in 3 b(i))and the n-buffer short resistance. The bipolar conduction only occurs when the anode junction (i.e. the base-emitter junction of the pnp transistor) become forward biased.

$I_{snap\text{-}back} \cdot Rs = 0.7V \rightarrow I_{snap\text{-}back} = 0.7/10 = 70mA.$

$V_{snap\text{-}back} = (Rch + R\ acc + R\ drfift) \cdot I_{snap\text{-}back} + 0.7\ V = (20 + 50)\ 0.07 + 0.7 = 5.6V$

The voltage drop on the channel is given by the channel resistance mul;tiplied by the snap-back-current = 1.4V. This is much smaller than the drive voltage V_G-V_T = 10 V which justifies that the MOS component is in the linear region and can be made equivalent to a resistor.

[35%]

(iii) The latch-up will occur when the npn transistor becomes active. This will happen when the base-emitter junction of the parasitic npn transistor becomes forward-baised.

The condition from the equivalent circuit shown see figure in 3 b(i)) is:

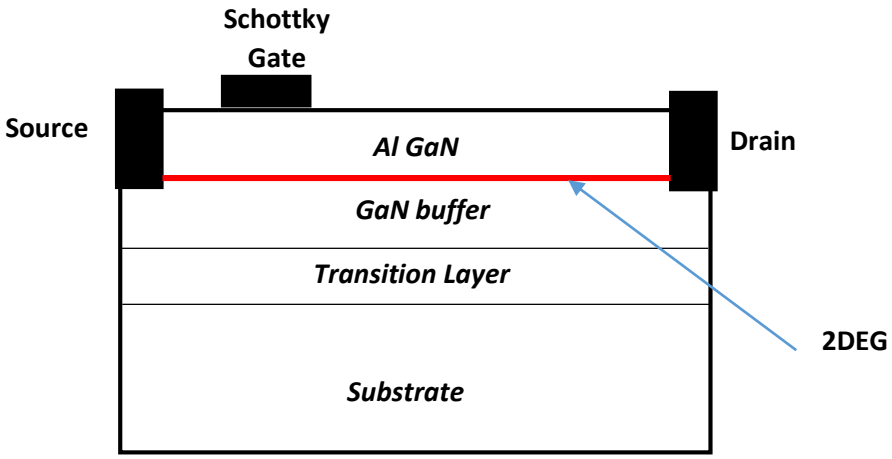
$\alpha_{pnp} \cdot I_A \cdot Rp = 0.7V \rightarrow I_A = 0.7/(0.3 \cdot 1) = 2.33\ A$

If the temepreature israised because of self-heating, then the voltage drop at which the forwar-biasing of the base-emitter junction of the npn transistor (between the n+ cathode and the p well) occurs, will frop with ~ 2mV/^{o}C. For a 50 ^{o}C rise, this drop is ~0.1 V. As reuslt the junction becomes forward biased at 0.6V instead of 0.7 V. Given this:

$I_A = 0.6/(0.3 \cdot 1) = 2\ A$

[20%]

4. The device is based on a Two Dimensional Electron gas (2DEG) formed between a GaN buffer and an AlGaN layer placed on top. The current flows from the source to the drain through the 2DEG layer. The gate modulates the flow of the electron current through the 2DEG and is used to turn on or turn off the device. Because the gate is based on a Schottky metal placed directly on the AlGaN, the device is normally-on with a negative threshold voltage. The device is therefore turned off or in the off-state when the gate potential applied to the gate with respect to the source is smaller (more negative) than the threshold voltage. In the off-state the device can block high voltages applied to the drain.

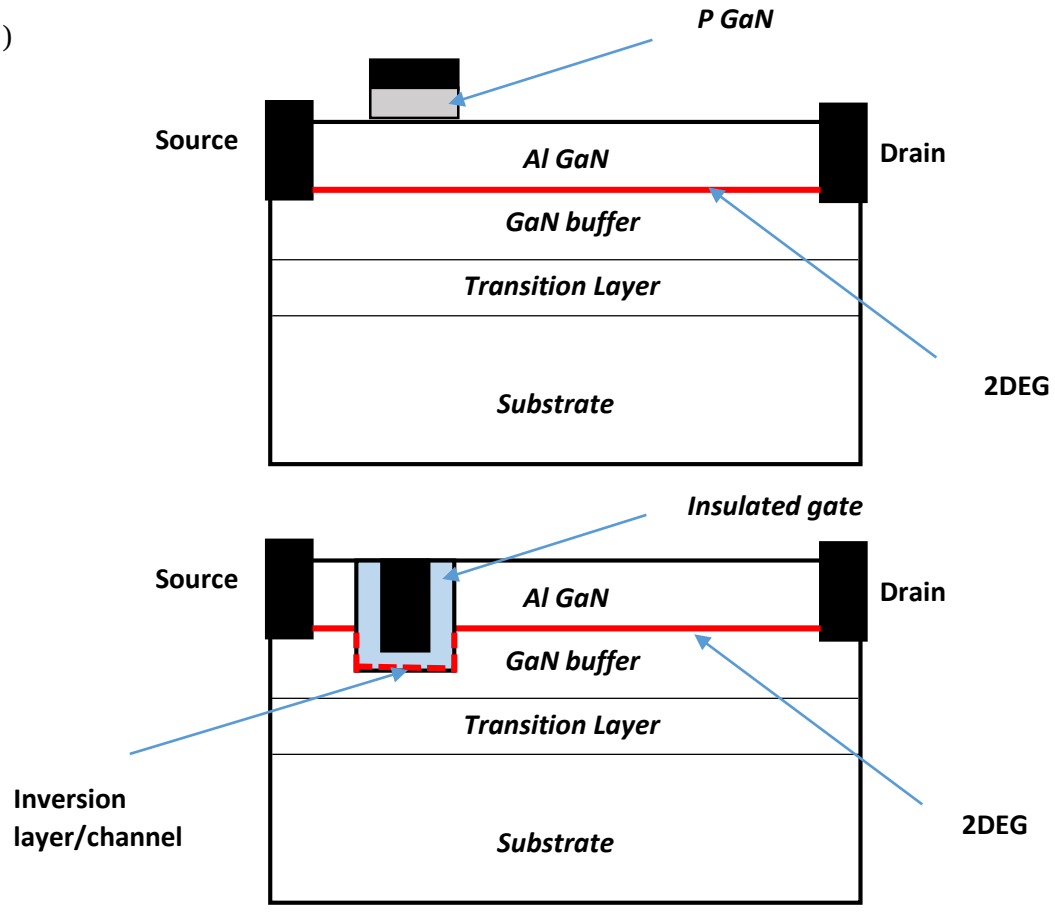


[25%]

(b) Increasing the gate to drain distance allows higher breakdown, as this relaxes the electric field between the gate and drain but results in higher on-state resistance. The speed will also be slower due to increase in the capacitances when the gate to drain incerases

[25%]

(c)



The two structures can deliver normally-off devices rather than normally-on. When the gate-source voltage is 0V both these structures deplete the channel under the gate as opposed to the Schottky gate structure that features a negative threshold voltage.

[25%]

(d) Advantage1 : GaN is wide bandgap material which offers much higher critical electric field than silicon. Hence the dimensions of a HEMT are much smaller for the same rated voltage. This results in much lower on-state resistance and potentially lower cost and cheaper packaging.

Advantage2: The GAN HEMT has much higher mobility in the 2DEG (close to 2000 $cm^2/(Vs)$) than the silicon. The maximum bulk/channel mobility in silicon is around to 1200 $cm^2/(Vs)$. As a result the GaN HEMT offers significantly lower on-state resistance and smaller form factor.

Advantage 3: The GaN device has easy access to all terminals because of lateral configuration. It is easier to co-package with a drive, protection or controller circuit.

Disadvantage 1: Initial cost of the wafers. The technology is still expensive as it requires GaN layers to be grown on silicon substrates.

Disadvantage 2: Because of the lateral configuration, the current capability is limited when compared to a vertical device. [25%]

Examiner's comments:

Question 1, on the SMPS design and calculation of losses for a SiC BJT was attempted by all candidates. This question was answered by all the candidates to a very high standard (14.7/20). It was pleasing to see that the candidates had good knowledge of SMPS systems and calculation of losses. Most of the candidates were able to calculate the instantaneous losses. The fact that the gain of a SiC BJT is higher than that of an equivalent Si BJT was answered well only be a few candidates

Question 2 was split into two parts (a) the latch up (b) parallel branches of MOSFETs. The question was attempted by all candidates with an average of 14.07/20 for undergraduates. The candidates answered very well this question. It was pleasing to see that all candidates understood the latch-up in IGBTs. Some candidates were confused buy equal source resistances and identical MOSFETs in the two branches and did not spot the symmetry and the fact that the two branches will see an identical current simplifying the question.

Question 3 was a typical device physics question where the candidates were asked to look at an anode shorted IGBT and calculate the latch-up. Only 4 candidates were able to draw a correct equivalent circuit and only one to calculate correctly the latch-up current and voltage. This was attempted by 5 candidates with an average 11/20 for undergraduates.

Question 4 was on GaN HEMTs. GaN HEMTs are now seen as the next generation of power devices replacing silicon in many applications. It was very pleasing to see that most of the candidates who attempted this question (9) were able to understand the different technologies available today in GaN and understand the benefits of GaN devices in comparison with silicon devices. Average 15.44/20