Version FU/2

EGT3
ENGINEERING TRIPOS PART IIB

Wednesday 5 May 2021 1.30 to 3.10

Module 4B2

POWER MICROELECTRONICS

Answer not more than ***three*** *questions.*

All questions carry the same number of marks.

The ***approximate*** *percentage of marks allocated to each part of a question is indicated in the right margin.*

Write your candidate number ***not*** *your name on the cover sheet and at the top of each answer sheet.*

STATIONERY REQUIREMENTS
Write on single-sided paper.

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed.
You are allowed access to the electronic version of the Engineering Data Books.

10 minutes reading time is allowed for this paper at the start of the exam.

The time taken for scanning/uploading answers is 15 minutes.

Your script is to be uploaded as a single consolidated pdf containing all answers.

1 (a) Explain the difference between the breakdown voltages BV_{CE0} and BV_{CB0} in a Bipolar Junction Transistor (BJT). Sketch the two breakdown characteristics of the BJT and explain the secondary breakdown effect. Can the secondary breakdown occur in a MOSFET or an IGBT? [20%]

(b) Fig. 1 shows the waveforms of a Silicon Carbide BJT switch in a simplified resistive switching circuit. The base resistance from the driver to the BJT is 1Ω. The switch operates at a switching frequency f = 100 kHz with a duty cycle D = 50%. The other parameters are: line voltage V_{dc} = 50 V, off-state leakage current I_{OFF} = 1 mA, on-state collector current I_C = 100 A, on-state base current I_B = 2 A, collector-emitter on-state voltage drop V_{CE} = 2 V, base-emitter on-state voltage drop V_{BE} = 2.5 V, turn-on delay time t_d = 0.5 μs, turn-on current rise time t_r = 0.1 μs, turn-off delay time t_s = 0.5 μs, turn-off current fall time t_f = 0.3 μs.

(i) Estimate the static, switching and total power losses in the switch. [30%]

(ii) Calculate the power loss due to the base current. [10%]

(iii) Draw schematically the structure of the BJT and explain its operation in the on-state. [10%]

(iv) Calculate the on-state current gain of the BJT and comment on this value compared to that of an equivalent silicon based BJT. [10%]

(v) Comment on the frequency of operation of the SiC BJT compared to that of a conventional silicon based BJT with similar voltage and current ratings [10%]

(vi) Why is the base-emitter voltage higher in SiC BJTs compared to that of a silicon based BJT? Is this advantageous? [10%]

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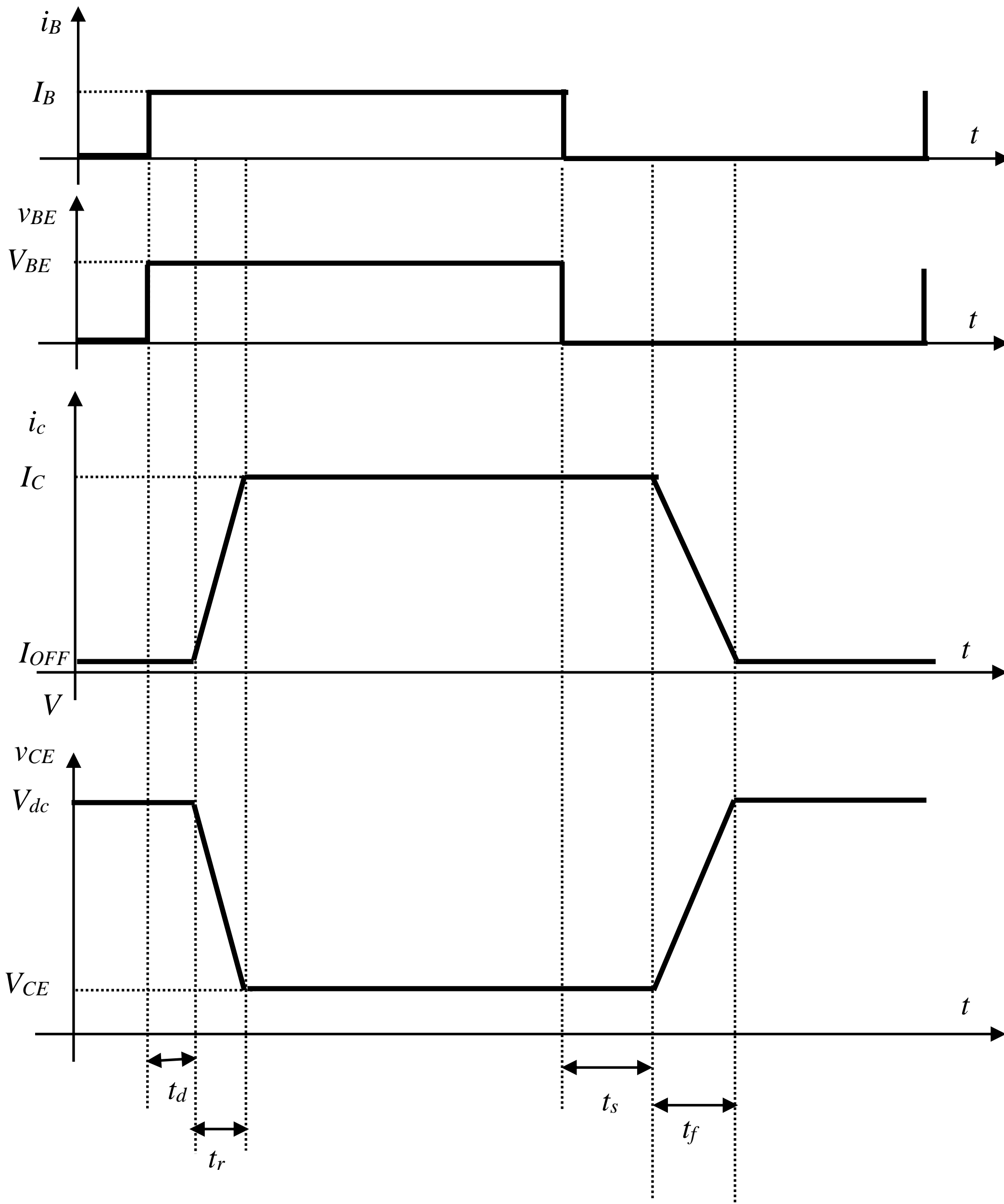

Figure 1

2 (a) Explain the latch-up effect in Insulated Gate Bipolar Transistors (IGBTs). Draw an IGBT equivalent circuit that includes the parasitic latch-up elements. Give two solutions to improve the latch-up immunity in IGBTs. [25%]

(b) Two high voltage MOSFETs M_1 and M_2 shown in Fig. 2 are operated in parallel. Two resistors R_1 and R_2 are placed in series with the sources of the two MOSFETs, M_1 and M_2, respectively.

(i) If the series resistances of R_1 and R_2 are equal, explain the mechanism by which the two series resistors help equal current sharing between the two MOSFETs in steady state conditions. [20%]

(ii) Propose modifications to the circuit in Fig. 2 to improve the current sharing in dynamic conditions. [25%]

(iii) In Fig. 2, R_A = 49 Ω, R_1 = 2 Ω, R_2 = 2 Ω, the gate potential of M_1, V_{G1} = 11 V, the gate potential of M_2, V_{G2} = 11 V and the line voltage, V_{CC} = 100 V. Both transistors have a threshold voltage, V_T = 1V. Assume that the MOSFETs operate in the linear region and each of their on-state resistance can be expressed as $Ron = 900/(V_{GS} - V_T)$, where V_{GS} is the potential drop between the gate and the source for each transistor. Determine the current flowing through each transistor. [30%]

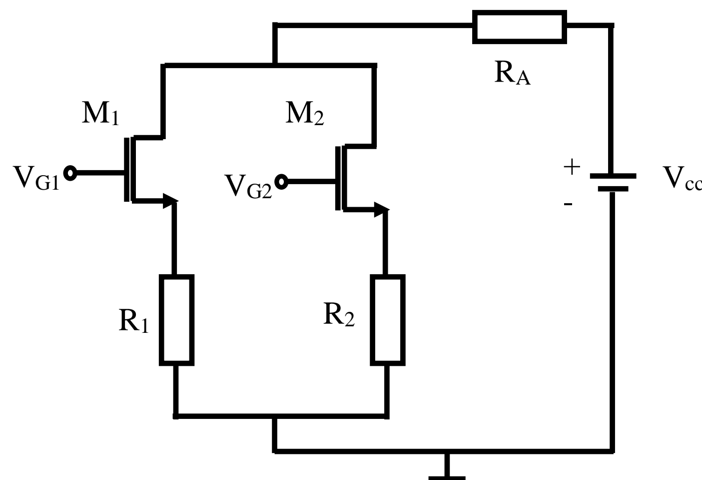

Figure 2

3 (a) Sketch the cross-section of an anode-shorted vertical trench IGBT structure. Describe the operation of the device highlighting the main advantages and disadvantages of this structure compared to a classical vertical IGBT. [25%]

(b) An anode shorted, vertical trench IGBT has an equivalent n-buffer short resistance (i.e. the resistance that appears in parallel with the base-emitter junction of the pnp transistor) of 10 Ω. The doping resistance of the drift layer, including the spreading resistance from the accumulation layer, is 50 Ω. The channel resistance including the accumulation layer resistance is 20 Ω. The effective gate voltage V_G - V_T = 10 V. The equivalent short resistance of the p-well (i.e. the resistance that appears in parallel with the base-emitter junction of the parasitic npn transistor) is 1 Ω. The effective current gain α_{pnp} when the device is in the normal operating on-state condition is 0.3.

(i) Draw the equivalent circuit of the device, including the parasitic npn transistor, the n-buffer short resistance and the p-well short resistance. [20%]

(ii) Find the snap-back voltage and current, where the device changes from a unipolar mode into a bipolar mode. State any assumptions made. [35%]

(iii) Find the latch-up current. Explain what would it happen if the device temperature is raised by 50 ^{o}C due to self-heating. State any assumptions made. [20%]

(TURN OVER

4 (a) Draw a Gallium-Nitride High Electron Mobility Transistor (GaN HEMT) based on a Schottky gate and explain its operation in the on-state, off-state, turn-on and turn-off modes. [25%]

(b) Explain all the operational consequences (and the associated trade-offs) of increasing or reducing the distance between the gate and the drain terminals in the GaN HEMT. [25%]

(c) Draw a GaN HEMT based on an insulated gate and a GaN HEMT based on a p-GaN gate. What are the advantages and disadvantages of these two HEMTs compared to a standard Schottky gate GaN HEMT? [25%]

(d) Give three advantages and two disadvantages of a GaN HEMT over a silicon power MOSFET for the same off-state voltage range, 600 V to 1.2 kV. [25%]

END OF PAPER

ENGINEERING TRIPOS PART IIB 2021
4B2 Numerical Solutions

Q1: (b) (i)*Total Losses = 134W*
On-State losses: 88 W, MOSFET, Turn-on switching losses = 9W, Turn-off losses: 37W
(ii) On-state base losses: 4.5W
(iv) Gain =50

Q2: (b) (iii) currents are equal in each branch = 0.5A

Q3: (b) (ii) $I_{snap\text{-}back}$ = 70mA.; $V_{snap\text{-}back}$ = 5.6V

(iii) I_A= 2.33A or for a 50C temperature rise I_A= 2A