Version FU/2

EGT3
ENGINEERING TRIPOS PART IIB

Monday 25 April 2022 2 to 3.40

Module 4B2

POWER MICROELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination room.

1. (a) Based on the physical properties of Silicon Carbide and Silicon, state the advantages of Silicon Carbide Power MOSFETs compared to Silicon Power MOSFETs. Why are there no Silicon Carbide Power MOSFET products rated below 100 V in the market? [20%]

(b) Fig. 1 shows the waveforms of a Silicon Carbide BJT switch in a simplified resistive switching circuit. The switch operates at a switching frequency f = 100 kHz with a duty cycle D = 50%. The other parameters are: line voltage V_{dc} = 50 V, off-state leakage current I_{OFF} = 1 mA, on-state collector current I_C = 100 A, on-state base current I_B = 2 A, collector-emitter on-state voltage drop V_{CE} = 2 V, base-emitter on-state voltage drop V_{BE} = 2.5 V, turn-on delay time t_d = 0.5 μs, turn-on current rise time t_r = 0.1 μs, turn-off delay time t_s = 0.5 μs, turn-off current fall time t_f = 0.3 μs. [40%]

(i) Estimate the static, switching and total power losses in the switch.

(ii) Calculate the power loss due to the base current. [10%]

(iii) Draw schematically the structure of the BJT transistor and explain its operation in the on-state. [20%]

(iv) Calculate the on-state current gain of the transistor and comment on this value compared to that of an equivalent silicon-based BJT. [10%]

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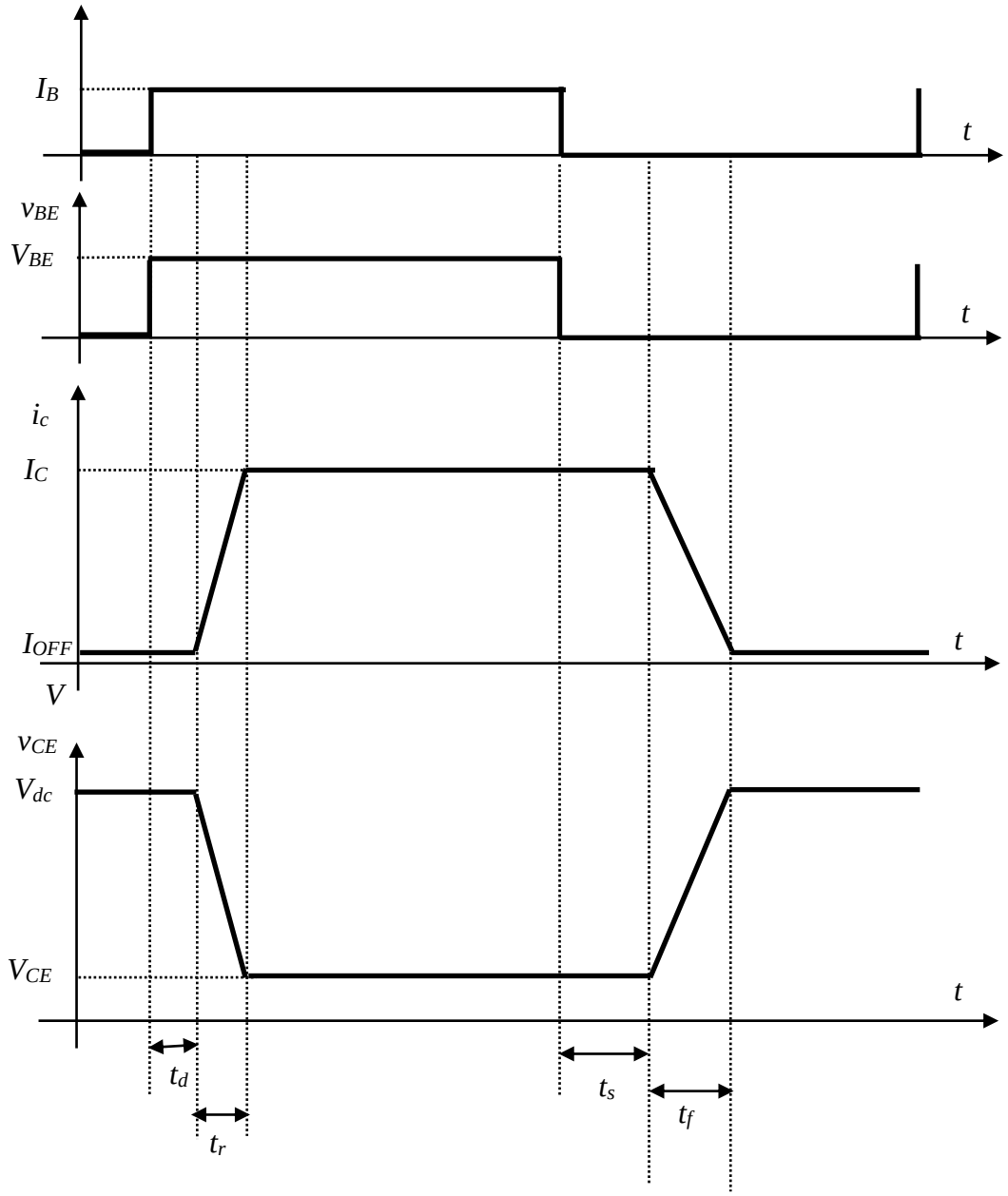

Fig.1

2 (a) (i) Draw the structure of the Cool MOS and explain its advantage in terms of the trade-off between the specific on-state resistance and the breakdown voltage. [20%]

(ii) Draw schematically a graph of the drain-source capacitances as a function of the blocking voltage for both the Cool MOS and a conventional Power MOSFET. Explain briefly the different behaviour of the two capacitances at low voltages and high voltages. [25%]

(b) (i) A power MOSFET and a Cool MOS are to be designed to have the same breakdown voltage V_{BR}. Assuming that the critical electric field, E_{cr} remains constant, independent of the doping level, find the optimal doping level and the optimum width of the drift region for the power MOSFET. What is the optimum width of the drift region for the Cool MOS to deliver the same V_{BR}? [25%]

(ii) Assume that the doping levels of the Cool MOS n-pillar and p-pillar are twenty and five times higher than the doping level of the drift region in the power MOSFET respectively. Find the relative decrease in the specific drift on-state resistance of the Cool MOS with respect to that of the Power MOSFET. [20%]

(iii) What are the benefits in reducing further the n-pillar and p-pillar widths in a Cool MOS? [10%]

For question 2 (b) you may assume the following equation in the calculation of the breakdown voltage

$$w = \left[\frac{2\varepsilon_r \varepsilon_0 V}{q} \frac{1}{N_D} \right]^{\frac{1}{2}}$$

where w is the depletion region width; N_D is the doping concentration of the drift region, V is the blocking voltage, q is the electronic charge and the other symbols have their usual meaning.

3 The structure in Fig. 2 is a vertical Silicon Carbide MOS controllable power device with a trench gate.

(a) Explain its operation during on-state, off-state, turn-on and turn-off. [30%]

(b) What is the specific role of the p+ layer placed under the trench gate? Should this layer be floating or connected to a terminal? What are the considerations in each case? [25%]

(c) Give two advantages and two disadvantages of this device compared to a conventional Silicon Carbide Trench Power MOSFET. [20%]

(d) Modify the device shown in Fig. 2 to operate as an Insulated Gate Bipolar Transistor (IGBT). What are the challenges, the benefits and the drawbacks of making an IGBT using Silicon Carbide? [25%]

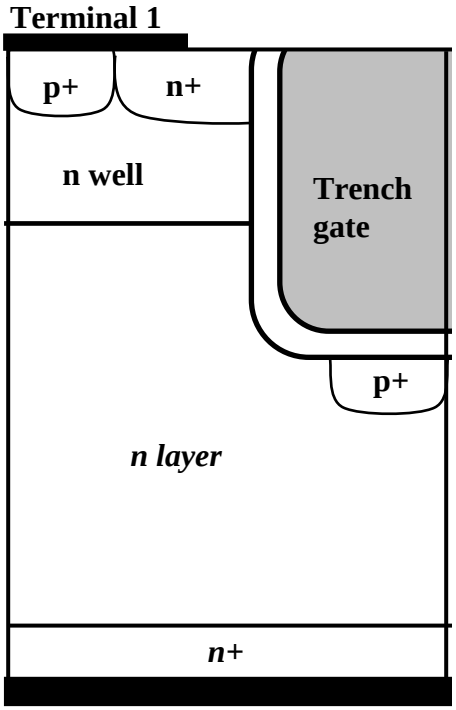

Fig. 2

4 Fig. 3 shows a CASCODE structure based on a low-voltage enhancement mode Silicon MOSFET and a high voltage depletion mode Gallium-Nitride High Electron Mobility Transistor (GaN HEMT).

(a) Draw the structure of a depletion mode GaN HEMT and briefly explain its operation in the on-state and off-state. [20%]

(b) Explain the operation of the CASCODE structure, during on-state, off-state, turn-on and turn-off modes. [30%]

(c) Give two benefits and two drawbacks of the CASCODE structure when compared to an enhancement mode GaN HEMT. [15%]

(d) Give two advantages and two disadvantages of a GaN HEMT over a Silicon Carbide power MOSFET for the same off-state voltage rating, 600 V. [15%]

(e) Explain the existence and the specific role of the diode shown in Fig. 3. [20%]

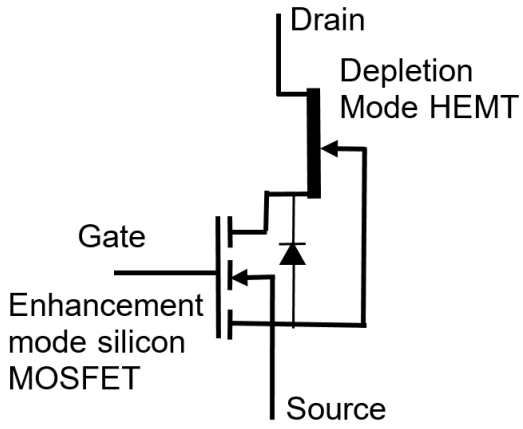

Fig. 3

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ENGINEERING TRIPOS PART IIB 2022
4B2 Numerical Solutions

Q1: (b) *Total Losses: 134 W* (On-State losses: 88W, Turn-on Losses: 9W, Turn-off losses : 37 W), The base losses: 2.5 W, the current gain I_C/I_B =50

Q2: (b) Cool MOS has ½ drift region compared to Conventional MOSFET

Rsp-Cool MOS/Rsp-MOSFET = (1/20) x 5 x (1/2) = 0.125